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Feasability Demonstration of The Vienna type Excitation System for Synchronous Generators

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CONTENTS

I. Abbreviations and acronyms

α	Firing angle for a thyristorbridge
B	Magnetic field strength
CCM/DCM	Continuously/Discontinuously conduction mode
d, D	duty cycle, average duty cycle
Δu_c	Voltage difference of the output capacitors
IGBT	Insulated-gate bipolar transistor
f_s	Frequency of supply
f_Δ	Switching-frequency
FPGA	Field Programmable Gate Array
HDBS	High-speed De-excitation for Brushless Synchronous machines
i_s	Mains phase currents
$i_{N,M}$	Neutral point current
μ	Switching angle in thyristorbridge
L_f	Inductance of field-windings
ψ_f	Rotorside magnetic flux
l	Active length of solonid
$\mu_{0/r}$	Magnetic permability of air/relative
L_s	Total input-inductance
M	Modulation index
MPC	Model-predictive control
N_r/N_s	Winding on the rotor/stator of the feeder
$N_{r,SG}/N_{s,SG}$	Winding on the rotor/stator of the SG
Q_x	Ideal switch x, e.g. two IGBT's in antiparalell.
pf	Power factor
PFC	Power Factor Corrected
PM	Permanent Magnet
PWM	Pulse width modulation
R_s	Total input-resistance
RPE	Rotating Power Electronics
S_x	State of switch x. '1' indicates a closed switch.
$\mathbf{S}$	Switching vector, e.g. $\mathbf{S} = [110]$ in sector 2
$\mathbf{S}_x$	Sector invariant switching vector , e.g. $\mathbf{S}_7$
SVM	Space vector modulation
THD	Total Harmonic Distortion
u_s	Mains phase voltages
u_{th}	Threshold voltage for a diode
u_d	Output voltage from the VR
U_{dm}	Applied demagnetization voltage
U_{BE}	Base-emitter voltage of an IGBT
$v_{\alpha\beta}$	Variable v in $\alpha\beta$-coordinates
v_x	Variable v for phase x where $x \in a, b, c$
V	Time invariant variabel v, rms or DC
$\underline{v}$	Phasor v
$\not{v}$	Not variable v. If $v = 1, \rightarrow \not{v} = 0$
$\vec{v}$	Vector v
v^*	The reference value of the variable v
v^1	Fundamental of the variable v
VR	Vienna rectifier
$\hat{v}$	Maximum value of the variable v
$\bar{v}$	Average value of the variable v
VI	Virtual Instrument, LabView filetype.

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Abstract—The operation of the Vienna rectifier has been analyzed and relevant literature on the rectifier has been reviewed. Furthermore, the Vienna rectifier in scope of rotating power electronics in brushless excitation has been discussed and found to be an viable option. The Vienna Rectifier have been simulated with the parameters from the Svante testrig in Matlab Simulink with satisfactorily results. A re-connection of the main windings is necessary. Also demagnetization-strategies and necessary modification to the Vienna Rectifier has been discussed and simulated. A demonstration of the Vienna Rectifier were build, but experimental results are remain qualitative due to practical issues with the demonstration rig. The control were designed in LabView Instruments and the workings of the control-scripts were confirmed.

The main challenge is comes from dealing with the large inductance from the mains winding on the rotating exciter, but this challenge may be overcome. Additional circuitry consisting of a chopper on the output and demagnetization resistor and switch should be added to ensure better controllability and demagnetization-capability.

II. Introduction

I n his PhD thesis *A New Paradigm for Large Brushless Hydrogenerators Advantages Beyond the Static System* [29], Jonas Nøland among other things scrutinized several different configurations of rotating power-electronics (RPE) in a prototype test rig situated at Uppsala University. Previous demonstrations clearly overlooked the Vienna Rectifier (VR) as a potential topology for excitation systems. This thesis will address this question with this test-rig specially in mind.

The excitation system of synchronous machines have recently experienced a new era of developments. Rotating power electronics as a means to excite the field windings of synchronous machines is a promising development in the mature field of electrical power-generation. Considering the improvements in the semiconductor technology and new possibilities for fast and flexible control, more complex topologies than the thyristor-bridge may be considered a realistic possibility. The issues related to rotating power electronics are not strictly electrical - also mechanical and thermal challenges as well as communication with the circuit must be met. Some of these issues will be addressed in this thesis; However, the main subject will be the electrical performance.

The VR is a power factor correcting boost-type rectifier that has been thoroughly analyzed and tested since it's emergence in the early 90's. Its high power density and proven reliability makes it a probable candidate for the brushless excitation scheme, in addition to possibly also the static excitation system. The workings of the Vienna is however not straight forward and will be described in depth in section III.

The VR will be simulated using Matlab Simulink/Simscape Power systems both in steady state and in transients. Rapid demagnetization and magnetization (field forcing) is one of the key qualities of the excitation topologies, and different suggestions will be scrutinized.

The VR is a commercially available product[20]. However, hands on experience is needed to be able to advice an optimal design for new applications, i.e., excitation systems. In this thesis, a downscaled demonstration-rig of the VR were built as to gather experience regarding building such prototype VR to pass on to design engineers or possibly later master-students finishing the project. This will also enable measurements over e.g. individual components and a flexibility that may not included in a commercial product. The demonstration rig will be described in section VI. The control will be written in LabView and implemented in a National Instruments (NI) control-board. To the authors best knowledge, there is not public available examples in either LabView or Simulink Powersystems of a working VR, and hopefully this thesis may be used as inspiration for engineers wanting to implement such a prototype for excitation purposes.

In the autumn of 2017 the author took a special course under the supervision of Jonas Nøland were the VR was initially considered. Partly to avoid overlap, PWM and other control-strategies that were considered in the special course, will not be discussed in this thesis. The report from the course is available for download [17]. Another reason why hysteresis-control were chosen is its simplicity.

A. Problem

One of the inspirations for considering the VR as topology is it's good track record in literature as well as the possibility to utilize the winding-inductance as filter-inductances. In traditional applications these are added and are a central design-aspect for the VR. In this application the input-inductances are a constraint rather than

a design-question in and of itself. The main issues that are attempted answered in this thesis are:

- May the VR be used as excitation topology in the scope of RPE, especially with Svante testrig in mind?
- Which, and in what manner, should necessary modifications to ensure demagnetization-strategies be applied?

Secondary tasks are:

- Estimate whether the necessary components (capacitors, IGBTs, diodes) are able to withstand the rotary forces that RPE demands or not.
- Build Matlab Simulink models modeling the VR in this application
- Build and control a small VR prototype to get insight in the construction of such a prototype.

III. THEORY

A. Fundamentals

1) The three-phase system: The power-system, and as a consequence also the VR, utilizes a three phase system. A three phase system can be written as:

$$
\begin{aligned}
u_a &= \hat{u_a} \sin(\omega t) \\
u_b &= \hat{u_b} \sin(\omega t - \frac{2\pi}{3}) \\
u_c &= \hat{u_c} \sin(\omega t + \frac{2\pi}{3}) \\
\omega &= 2\pi f
\end{aligned}
\tag{1}
$$

In a *balanced* three-phase system $\hat{u_a} = \hat{u_b} = \hat{u_c}$. In many applications, the VR being one of them, it is instructive to describe the three phase-system in the complex plane and describe them by a single phasor. This is done by a Clark/Park transform

$$
\underline{u_{\alpha\beta0}} = \begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = K\vec{C}\vec{u_{xN}} = K \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}
\tag{2}
$$

In 2 the scaling-factor is mostly chosen as $K = \frac{2}{3}$, resulting in a *amplitude-invariant* transformation. That is, $|u_{u_{\alpha\beta0}}| = \hat{u_{abc}}$. As a consequence the power in the system is not equal. To get the *power-invariant* transformation $K = \sqrt{\frac{2}{3}}$. In this thesis the amplitude-invariant transform will be used.

2) IGBT: A simplified schematic of an IGBT is illustrated in Fig. 1. The physical structure of the IGBT is shown in 15, where the rotary centrifugal forces are adressed For a schematic view of the doping-layer is shown in the discussion regarding the rotary forces on an IGBT.

The red slope marked in 2 is to indicates what kind of area one operates the devices in power electronics. The goal is to supply an gate-emitter voltage that ensures that the device never goes into saturation. In other words, that it operates in the ohmic area. Ideally, it should conduct
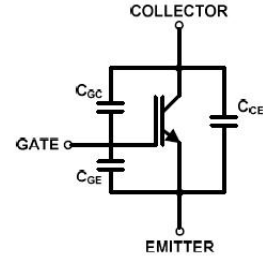

Fig. 1. The illustration is taken from [33] where also much of the inspiration for this section were found.
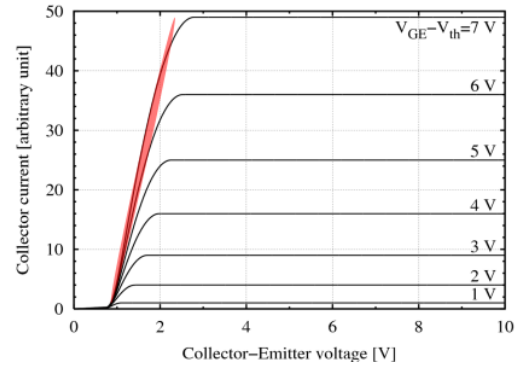

Fig. 2. The characteristic of an IGBT [7]. The red area is added by the author.

current with a low forward voltage drop, i.e., the low-ohmic region. The values in the chart is not representative for the switches used in this thesis.

3) Drivers: Important for the discussion in this thesis is the gate-emitter capacitance, C_{GE}. To turn the IGBT fully on this need to be charged up to $U_{GE,th}$. Micro controllers and similar devices seldom have the current-capability (if they can supply $U_{GE,th}$ at all) to charge and thus turn on the IGBT on satisfactory speeds. Therefore external drive circuity is employed to ensure satisfactory operation of the IGBT. In every case a gate resistor should be employed to limit the turn-on current. The peak-current can be estimated as [33]:

$$
I_p = \frac{V_{on} - V_{off}}{R_g + R_{internal}}
\tag{3}
$$

There are several online tools and guidelines[45], [47], [40] regarding the selection of parameters and driver-types. There are several techniques to design the drive circuitry [41] depending on the needs for isolation, whether the emitter is tied to ground or not and many other considerations.

4) Capacitors and inductors: Despite fundamental differs in construction, these two components may be described together as twins. The defining equations describing the components are shown below on integral and derivative forms:

$$\frac{u_c}{dt} = \frac{1}{C} i_C$$
$$\int_{t_0}^{t} i_C = C u_C + U_{C,0}$$
(4)

The physical explanation of of eq. 4 is easies described thought the integral-form: As charge (the time-derivative of current) accumulates/is being removed from the sides of the capacitors, they will produce an electrostatic-field across the capacitor, causing a charging up to a voltage. Capacitance, as well as inductance, is component-specific property.

$$\frac{i_L}{dt} = \frac{1}{L} U_L$$
$$\int_{t_0}^{t} u_L = i_L L$$
(5)

A current through a conductor produces a magnetic field. If the conductor is correctly wound into a coil around a material with large magnetic permeability, an substantial magnetic field may be produced (and upheld) by the current. If the current sinks, the magnetic field will experience weakening. According to Faraday's law this will induce a voltage over the coil, containing the current. The current will be reduced slower, lagging the applied voltage. The same mechanism applies for increasing of the current in the coil, according to Lenz' law.

5) Harmonies and THD: In the field of power-electronics, the currents and voltages aren't necessarily smooth sine-forms. To describe these, they are described as the sum of several sine- and cosine waves with different amplitude and frequency. This is formulated in complex form for a periodical function f(t)

$$f(t) = \sum_{-\infty}^{\infty} c_n e^{\frac{i 2 \pi n t}{T}}$$
$$c_n = \frac{1}{T} \int_{-T/2}^{T/2} f(t) e^{\frac{i 2 \pi n t}{T}} dt$$
$$n = 0, \pm 1, \pm 2, ...$$
(6)

where T is the period of the signal. An illustration using Matlabs FFT (fast fourier transform) function illustrating how such a signal can be described is shown in Fig. 3

The signal with $n = 1$ is the fundamental. Total Harmonic Distortion (THD) is a measure of how distorted (non-sinusoidal) the signal is:

$$THD = \frac{\sqrt{U_2^2 + U_3^2 + U_4^2 ...}}{U_1}$$
(7)

where U_n describes the rms-value of the n-th harmony of the signal U. In this thesis the power factor of non-sinusoidal currents are central. This is related to THD through the power factor of the the fundamental, pf^1.

$$pf = \frac{1}{\sqrt{1 + THD^2}} pf^1$$
(8)

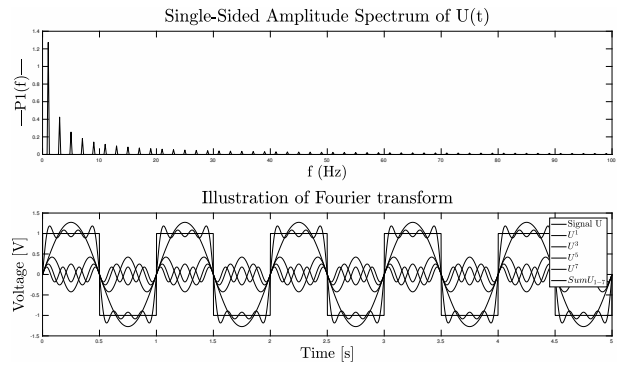The calculation of THD and pf in these simulations will be done through Matlab functions.

Fig. 3. The first harmonies and the sums thereof taken from a square signal. The summation shows that for such a signal, the lower harmonies alone can describe it quite good. The upper plot shows the frequency-spectrum. Note that the signal only contains harmonies of the order 1, 3, 5... This is due to the odd nature (u(-t) = -u(t)) of the signal.

B. The rotor-field in a synchronous generator

1) Static versus brushless excitation: The earlier methods for excitation of synchronous machines has been;

- Permanent magnets (PMs) with no field regulation on the rotating frame
- Non-salient rotor and salient stator
  - Fed from the grid
  - Excited from auxiliary source

The latter options offers many advantages over the former and is also the typical choice for direct on line (DOL) connected synchronous machines. The ability to control the rotor magnetic field makes the machine viable to regulate the flow of reactive power to the grid as well as reacting dynamically to faults in the grid. In the case of fault such as disconnection of other generators and subsequence voltage drop in the grid, the machine may increase i_f and thus Ψ_f to a) avoid falling out of synchronizity b) Keeping the power-balance and maintain frequency in the grid. c) Ability to demagnetize itself to avoid the dangerous effects of internal faults in the machine. A thorough explenation of the workings of the synchronous machine can be found in classic texbooks such as [23]. The main drawback in this scheme is the need to transfer current to the field winding through (usually) carbon brushes. Due to wear and tear from the mechanical stresses these are subjected to, they contribute a large deal to the maintenance of the machine. Further drawbacks using brushes are dust from the brushes which can interfere with the rest of the machine and a slight voltage drop over the brushes.

The modern, more robust excitation system transfers energy to the field winding through induction as seen in Fig. 4. The conventional static system is shown in Fig. 5

Instead of the chopper one may use, e.g. a thyristor-bridge - the main concept is that through controlling the voltage over the field winding, one controls the current and thus also the magnetic field.
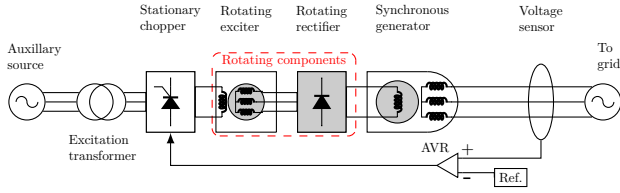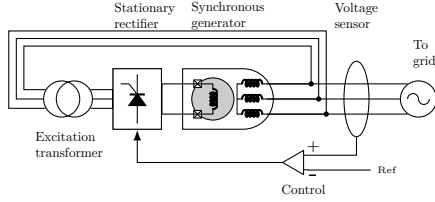
Fig. 4. Conventional, brushless excitation

Fig. 5. Conventional, static excitation

2) Open-circuit field winding as a RL-load: The field winding can be analyzed as shown in Fig. 6.
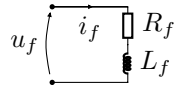

Fig. 6. The field winding ignoring the effect of mutual inductance in the open-circuit conditions of the stator

$$
\begin{aligned}
U_f &= i_f R_f + \frac{di_f}{dt} L_f \\
I_f &= \frac{U_f}{R_f}
\end{aligned}
\tag{9}
$$

The magnetic field produced by i_f is given by eq. (10)

$$
\Psi_f = i_f L_f \tag{10}
$$

The magnetic field produced by the rotor is magnetically linked with the one from the stator windings.

The solution to the first order differential eq. (9) is

$$
\begin{aligned}
i_f &= I_f + Ce^{\frac{-t}{\tau}} \\
T'_{do} &= \frac{L_f}{R_f}
\end{aligned}
\tag{11}
$$

I_f is in other words the DC-component of the steady state field current, assuming constant U_f. If one were to consider the mutual inductance the time-constant for the RL-load would become[37];

$$
L_f* = \frac{L_f - (M_f^2/L_d)}{R_f} \tag{12}
$$

where M_f is the mutual inductance between stator and rotor and L_d is the stator-winding direct-axis inductance. For the sake of simplicity the simplification $L_f* \approx L_f$ for the rest of the analysis, but must of course taken into consideration when dimensioning the actual rectification system.

Rather than using a passive diode bridge as shown in Fig.

4, an active circuit like the VR or a thyristor bridge on the rotor may be used. The stator winding of the excitation system may be fed from a stationary diode bridge feeding an armature-winding or PMs as shown in Fig. 7.
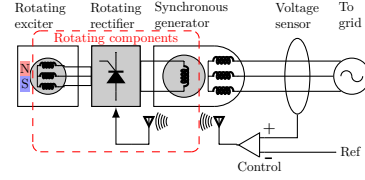

Fig. 7. Excitation using an activ rectifier and PM exitation on the stator of the exciter.

3) Pole configuration: It may be fortunate to increase the frequency on the exciter-mains. This has to advantages:

1) Slightly faster demagnetization using a thyristor-bridge
2) Smaller current-ripple on the output
3) Smaller filter-inductance is needed → Smaller volume used by power-electronics on rotor.

In advantage (1) an ideal thyristor bridge can go from maximum to the minimum voltage in:

$$
T_{thy,max \to min} = \frac{1}{6f_s} \tag{13}
$$

which shows how the increasing the supply frequency may improve the transient capacity of the thyristorbridge.

For a typical electrical machine, is the frequency on the mains is [52];

$$
f_s = \frac{\omega_{mec}}{8\pi} P_s P_r \tag{14}
$$

where P is the number of poles on the stator and rotor respectively.

4) Main windings inductance: Due to the crucial effect L_s may have on the operation of the VRs operation some basic considerations of the mains-windings inductans is necessary. For an ideal solonoid, the inductance can be formulated as

$$
L = \frac{\mu_0 \mu_r N^2 A}{l} \tag{15}
$$

Considering the field winding as such, A can be considered almost given from the mechanical constraints on the rotor. N may however be varied more easily by sectioning the available space designated for the windings into several windings. As a consequence the cross-section for each conductor has to be reduced proportional to N. Keeping series connections for all the conductors making up the field windings the length of conductor that the field current passes through also increases proportional to N. Since the resistance of a conductor is given by:

$$
R = \frac{\rho l}{A_c} \tag{16}
$$

where ρ is a material constant, l is the length of the conductor and A_c is the cross-section.

$$R_f \propto N^2 \rightarrow$$
$$R_f \propto L_f^4 \rightarrow \qquad (17)$$
$$U_f \propto L_f^4$$

Here it is assumed that the "new section" of windings is connected in series with the first one, in effect increasing the total length l as well as reducing the cross-section A_c. The last step in eq. (17) is assuming steady field current and drawing on eq. (9).

The induced voltage in the mains-winding is given by

$$\varepsilon = -N\frac{d\Psi}{dt} = -N\frac{d(BA)}{dt} \approx -NB\frac{dA}{dt} \qquad (18)$$

The last approximation in eq. (18) can be made since we're in this application is considering a stationary magnetic field on the stator supplying a constant field. The perpendicular cross-section between the coil and the magnetic field A is changing with the rotation of the rotor and coil. In the case of electric magnetization on the stator Amperes law governs approximation for a long solonoid is proportional with the current-magnitude:

$$B \propto Nl\mu_r I \qquad (19)$$

In the case of PMs, the magnetic field is given by the PMs properties. In addition comes considerations regarding air-gap, angle of windings, winding-configurations and so forth, but will be left out of this discussion.

Ideally, $\hat{B} \approx 1T$ due to saturation effect usually comes into play for materials used in stator-teeth around $1.5-2T$.

If one were to reduce the inductance of the stator coil the most straight forward measure is to reduce the number of coils. But one would in turn get an reduction in the induced voltage according to:

$$\frac{\Delta_N \varepsilon}{\Delta_N L_s} = \frac{1}{2} \qquad (20)$$

In other words, a 25% reduction in inductance due to fewer windings would result in a 50% reduction of induced voltage.

The losses in the windings determining are mainly[41]:
- Copper losses from ohmic losses in the winding. $P_c \propto i^2 R$
- Iron losses
  - Hysteresis-losses from hysteresis-loop in magnetization-demagnetization, $P_h \propto u^a f^b$
  - Core losses from induced eddy-currents, also $P_{eddy} \propto u^2 f^2$

where i is the current in the winding, u is the induced voltage in the winding, a and b are material-specific constants.

From the above list it clear that the windings are determined by the current and voltage independently. Therefore such a rating is dimensioned after apparent power S. Achieving $P = S \rightarrow pf = 1$ entails in other words the full utilization of the windings rating.

C. Magnetization and demagnetization

In this thesis, magnetization and demagnetization will refer to the transient response of the excitation system. Magnetization refers to a step in reference I_f^* from a running, synchronous state, not at startup of the generator. In this case a different approach must be taken to ensure correct grid synchronization and so forth.

1) Magnetization: In the case of e.g. a line to ground fault, the grid voltage in nearby area will be greatly reduced. The magnitude will wary with distance to the fault, type of fault (single pole or not, resistance to ground etc.), but will in many cases be of such an magnitude that it may cause a problem for the generator with synchronization with the grid. A review of the effects of generator and grid parameters on these kind of faults can be found in [42]. During a low-voltage ride-through (LVRT) fault there are mainly two issues; a) Faulty tripping of protection-systems causing the generator to be disconnected possibly contributing to an increase of the fault and b) Weakened magnetic link between stator and rotor due to fall in stator-voltage leads to runaway speed and loss of synchronization of the synchronous generator. Only b) and measures taken on the generator-side is in scope of this thesis. There are many possible measures that can be made [43]. The valve action is typical too slow to react in time, but the excitation system can react in the matter of tens of milliseconds. An increase in I_f leads to a stronger magnetic coupling.

The transient behavior of synchronous generators under FRT is regulated in mostly national grid codes. In Norway, Statnett is responsible for these and are currently working on implementing EU-regulations on this field that harmonises the grid codes somewhat[1]. In fig. 8, the fault are cleared at t_{clear} and the curve shows the rising terminal-voltage after clearance.
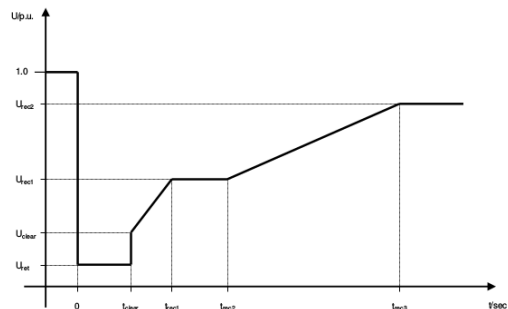

Fig. 8. A typical curve for required terminal-voltages after a fault. [1]

What for the excitation system goes, it is the ceiling voltage, that is how much and how fast U_f may be incresed $U_f[pu]$ that is regulated in the grid codes rather than i_f. The Norwegian TSO Statnett is demanding voltage of $2U_{f,n}$ over ten seconds, [32] and also dimensioning of the
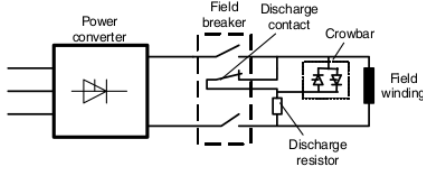
Fig. 9. The classical way of demagnetization using DC-breakers [46]

Fig. 10. Using AC-side breakers [46]

system to bare $2I_{f,n}$ over ten seconds. For the application of the Vienna this implies that a comparing quality is how fast and how much the topology is capable of increasing U_f.

In the conventional topology shown in fig. 4 this is achieved by controlling the stationary chopper or the firing angle of a thyristor bridge in its place. In most cases [29], the "auxillary source" in the fig. really is the grid. In this case the excitation-system would be rather exposed to a low voltage fault since it also would limit the available voltage at the stationary excitation-topology's terminals and thus U_f. Several other topologies [11][39] have been suggested with fast magnetization in mind. Using permanent magnets instead of an electromagnet controlled by stationary power electronics on the stator would mitigate this problem, but again demand RPE to regulate U_f.

2) Demagnetization: The need for good transient qualities of the excitation system is motivated by the same aspects as magnetization. From at regulatory view the rotor-field must be able to vary in response to varying mechanical power, and to change the reactive power delivered from the machine. As a safety mechanism the field must be possible to shut down very rapidly in case of faults that warrants a rapid seizure of the power delivered to the stator-windings. Such faults can be earths on stator side, flash over in the field winding or other electrical errors on the rotor side. An excellent review of demagnetization systems is found in [46].

As seen in fig. 9, the demagnetization system consists of three (four) parts;

(a) Power converter that may supply negative field voltage (e.g. thyristorbridge)
(b) Field breakers to disconnect the field winding from field voltage
(c) Discharge resistor in which the energy stored in the field windings magnetic field is dissepated.
(d) A crowbar circuit protecting the field winding from over-voltages.

Discussing the VR, especially the necessary modifications necessary to achive a) is of interest since the VR doesn't originally allow reverse power-flow. Breaking the DC-current will necessarily lead to the formation of an arc, which is the reason for the extra discharge breaker that ensures commutation of the current to the RL-circuit consisting of R_{dm} and L_f. In many cases a voltage-dependent
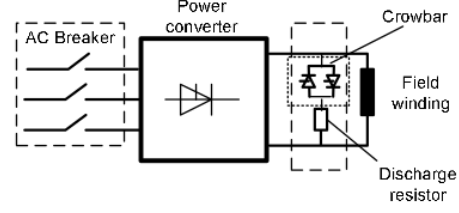
non-linear resistor is used for R_{dm}. This is made out of semi conducting material and increase the resistance with increased voltage. In this way the voltage over the field winding is kept low (high voltage reduces the resistance and thus lowers the voltage thorough current surge).

Breaker on the AC-side of the converter has also been used as shown in fig. 10. Altought this leads to a much simpler breaking of the current due to the utilization of the zero-crossings, special considerations have to be taken regarding longer arcing times and three phase faults at the stator. The more mechanical compact realization of the AC-breaker is a strong argument for the utilization of these in RPE since space is a constraint.

The effects of $a)$ and c can be described mathematical straight forward. Observing fig. 6 again, $a)$ can be described as supplying a negative $u_f = -|U_{dm}|$. Setting $i_f(0) = I_f$, the solution of the eq. (11) will be;

$$i_f = (I_f + \frac{|U_{dm}|}{R_f})e^{-\frac{t}{\tau}} - \frac{|U_dm|}{R_f} \tag{21}$$

$d)$ is equivalent to setting $U_f = 0$ and introducing the demagnetization resistance R_{dm} into the circuit. The solution then becomes;

$$i_f = I_f e^{-\frac{t}{\tau_{dm}}}$$
$$\tau_{dm} = \frac{L_f}{R_f + R_{dm}} \tag{22}$$

Writing the expressions with base quantities,

$$I_{f,b} = I_f$$
$$R_b = R_f$$
$$L_b = L_f \tag{23}$$
$$t_b = \frac{L_{f,b}}{R_{f,b}}$$

gives relative eq. from (21) and (22),

$$i_{f,r} = e^{-t_r(1+R_r)}$$
$$R_r = \frac{R_{dm}}{R_f} \tag{24}$$

$$U_r = \frac{|U_{dm}|}{U_f} \tag{25}$$
$$i_{f,r} = (1 + U_r)e^{-t_r} - U_r$$

Figure 11 illustrates eq. (24), also with the relative power dissipated in the demagnetization resistance.

$$P_{dm,r} = i_{f,r}^2 R_r \tag{26}$$

The field winding is dimensioned for full-load current, but this must be heeded when choosing demagnetization resistor. Equation (25) is illustrated in fig. 12 where only U_r is varied.
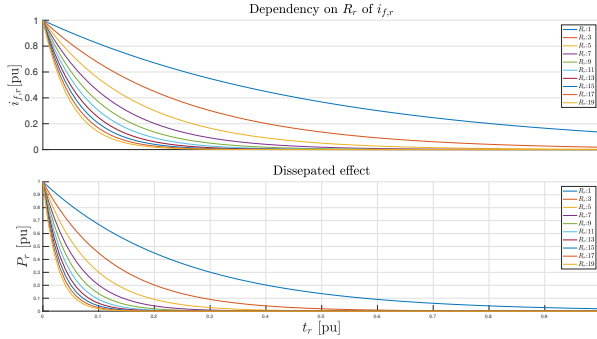

Fig. 11. The dissipated amount of power falls exponentiatial relative to $i_{f,r}$. The effect of increasing $R_r : 1 \to 3$ is more expressed than e.g. $R_r : 17 \to 19$.
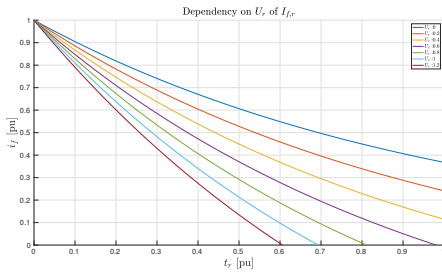

Fig. 12. Note that using $U_r = \frac{|U_{dm}|}{U_f} = 0 \to U_{dm} = 0$ results in simple demagnetization through field resistor with time constant τ and $i_{f,r}(1) = 37\% I_f$

D. Demagnetization with RPE

Common practice for conventional brushless excitation fail to include a discharge resistance and so forth since a commutation link to the rotor that can fire a demagnetize signal and switch over to the demagnetize-circuit isn't in place. In the conventional brushless excitation scheme shown in fig. 4 there is no breakers, AC or DC on the rotor at all. During demagnetization the statorside excitation is turned of. In addition to the large time constant given in eq.s (11), the effect of the stator main windings will also come into play. Due to the winding-inductance the rotor-mains current cannot collapse immediately and contribute to the slow reduction of i_f. Notable this contribution is small since $\frac{L_s}{L_f} << 1$ and has a much smaller time constant than the field-winding. A solution to this obvious drawback of brushless magnetization is presented in the series of papers [34], [37] and [38]. This configuration will be referred to as High-speed De-excitation for Brushless Synchronous machines (HDBS)

In fig. 13, the control circuit senses U_f. The rapid reduction of I_f and as a consequence the current into the
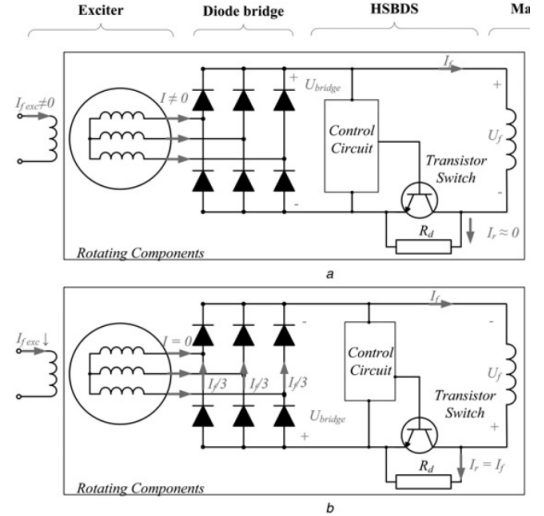

Fig. 13. A self-triggering demagnetization mechanism. [34]

diode bridge is not explicitly described in the research, but may e.g. be achived through a DC-breaker on the stator side. In an event where demagnetization is needed, the breakers on the stator feeding the rotor-mains will be triggered. With no voltage provided from the diode-bridge, the current in the field winding will fall and the polarity across the field winding will switch. This is the triggering signal for the control-circuitry that subsequently switches of Q_1 in fig. 13. This forces the current through the demagnetization-resistance instead, leading to a demagnetization with the qualities described in eq. (22).

PM stator magnetization of the exciter requires that breakers necessarily needs to be placed on the rotor, either on the DC or AC side. If the nature of the system (e.g. very safe operations, protection of the stator side) warrants it, one could go without breakers altogether as in conventional brushless system. But as the previous discussion has highlighted, this at least demands an power-converter that is able to supply negative field voltage so that the constant rotor mains-voltage can be used to reduce the time-constant of the demagnetization.

Excitation $\to$	PMs	EMs
Affected of stator voltage dip	No	Yes, but not instantly
Breakers	Rotor	Stator
Alt. to reverse powerflow	Breakers	Extra demag circuit

TABLE I: Consequences for stator magnetization. In the EMs case it is given that the excitations takes power from the grid.

E. Mechanical challenges with RPE

Rotating power electronics (RPE) needs to achive a high level of reliability and be relatively maintenance free to be a worth competitor to the static system using brushes. RPE is using other components than a diode bridge is not yet common in the industry and the experience regarding the mechanical effects on the power electronics are limited. In such a critical application as excitation, it is key that the components can stand the rotary forces over time. An illustration of the forces affecting a single device placed on the rotor (which is considered lying parallel with the ground) can be seen in fig. 14
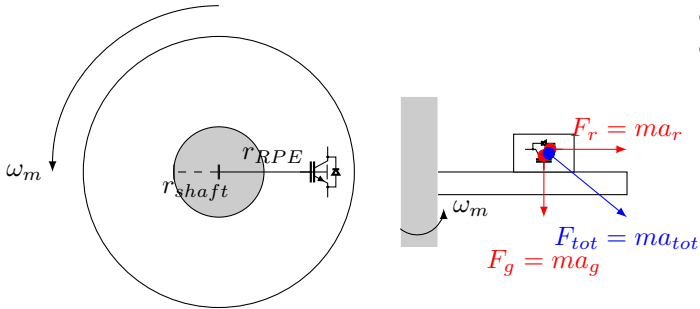

Fig. 14. The placement of the device is critical for the forces affecting it.

In fig. 14 F_g designates the gravitational forces ($F_g = G$) and F_r the apparent rotary forces. ω_m is the mechanical, angular velocity and the grey area designates the shaft of the generator. For most applications, $a_g << a_r$.

$$a_r = \omega^2 r \qquad (27)$$

This can be seen from eq. (27) and the fact that even for relatively small rotational speed ($400\,\text{rpm}$) and RPE very close ($10cm$) to the axis, the gravitational forces will be an order of magnitude lower than the once from the rotating movement.

The forces acting on the RPE will be both shear and normal forces if the PCB is placed perpendicular to the shaft and only secured thought soldering, either punch-through or surface mounted.

1) IGBTs: Modeling of the expected overall lifetime of a semiconductor power-module is a science in itself and is usually conducted by accelerated cycling test where both turn on/off and temperature cycling is used. The most common failures are bond wire fatigue/lift off, issues such as cracking at the solder-points and cracking of substrate. A cause for these failures may often be different Coefficient of thermal expansion which leads to internal stress as the transistor expands as a consequence from heating[22]. With RPE the additional stress that must be considered are not internal, but from the large rotary forces.

Rotating diodes for excitation purposes have been applied with great results [54]. The question remains regarding the considerations that must be taken when choosing capacitors and IGBTs. Barring the life-time issues, pressure applied to an IGBT may affect the characteristics

of the semiconductor. It were shown in [8] and [26] that pressure on a IGBT or MOSFET would affect parameters as transconductance, saturation current and v_{th}. The direction of the pressure relative to the current-flow is key. For illustration a cross-section of an IGBT is shown in fig. 15. In [8], it was shown that compressive stresses in the Y-direction reduced the saturation current and in [6] that compressive stress in the X-direction didn't effect the saturation current notably. As both papers states, the crystalline structure of the IGBT will determine the mechanical structures of the semiconductor. In addition, [6] shows that by knowing the crystalline orientation aligning the semiconductor correctly relative to the radi of the circular motion one may reduce the effect of saturation-currents.
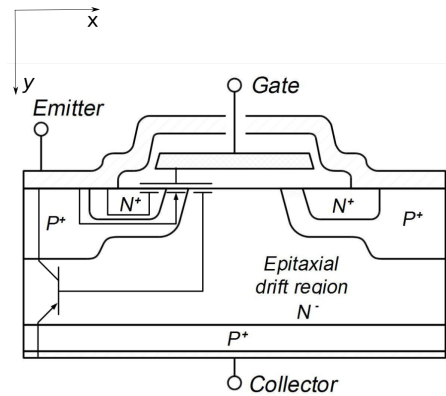

Fig. 15. A schematic view of an IGBT[51].

It should be noted that the size of the IGBTs and crystaline structure are different across the studies and from the components used in an RPE-application. The pressure that were applied were several MPAs However, comparing the results may give an indication on where the issues may arise. A simpler and probably safer solution is dimension the gate driver such that the IGBT will turn safely on and of also with modified saturation currents. At Sintef there have been conducted considerable research regarding press-packed IGBTs and film capacitors subjected to high pressure under water. Summary of the early results can be found in [18] and more detailed modeling and test-results for press-packed IGBTs in [35]. Press packed IGBTs were subjected to pressures up to clamping pressure up to $4000N$ and it was found that "low influence on the electrical behavior of the system in the range of rated current". Both a special-designed drivers and press-packed IGBT-modules were subjected to 100 and 300 bar liquid pressure. Also an off the shelf driver were testet on also lower pressures. Even thought the non-modified components suffered somewhat already in the 100 bar-test, they still performed.

Taking e.g. MII 200-12 A4 IGBT array from IXYS with $m = 250g, A = 6, 8e - 3m^3$ at $n1500\,\text{rpm}$ and mounting $30cm$ from the center of the shaft the maximum pressure experienced of the array at the mounting (perpendicular to a_r) is $\approx 270kPa = 2, 7bar$ using eq. (27). This indicates

that the rotary forces will not effect the electrical characteristics of the IGBTs, but as mentioned this should be tested with industry application in mind.

2) Capacitors: Sintef has also tested power capacitors in the same manner as press packed IGBTs with in general the same results. Electrolytic capacitors in the driver were the component which failed during high-pressure tests. The master thesis [48] is treating this research and results closer. Although having a large capacitance, this is one indication why wet-electrolyte capacitors should not be used in RPE. Another aspect is that the viscous gel in these components may be drained from one side to the other of the capacitor to the other during prolonged rotation. Using solid polymer would mitigate this danger, but limit the application regarding some demagnetization-strategies since it cannot be reversed polarized. Film- or ceramic capacitors seems to be the ideal choice on this background.

As goes for both the case of capacitors and IGBTs it must be noted that the mechanical stress these components have been subjugated to in the above mentioned research differs not only in magnitude, but also in what manner it is applied, from what would be the case with RPE. Since no research were found directly testing such components on a generator shaft, these results may indicate the expected behavior. Further research is needed, but from these results it seems that using press-packed IGBTs and film capacitors there should be no issues with the components in the RPE application.

Solder-points can also be a weak-spot for e.g. surface mounted ceramic capacitors[36].

F. Active rectification

In most applications of brushless excitation, thyristor-bridge is used to deliver the regulated voltage to the field winding of the machine as seen in Fig. 4. Even though considered a robust solution, one of the issues is that of regulated powerfactor (pf). In an ideal thyristorbridge, the output voltage is given by;

$$\bar{u}_d = \frac{3}{\pi}\hat{u}_s(\cos\alpha - \frac{\omega L_s i_d}{\hat{u}_s})$$ (28)

As shown in textbooks such as [41], the firing angle reduces the pf at the input of the rectifier. In addition, the current form is distorted to an non-sinusoidal form and in the process increasing THD thus high-frequency EMI. Since excitation demands variable output voltage, this means possibly over-dimensioning both of the rotorside mains-windings to deal with the maximum apparent power delivered for probable levels of u_d^*. If $S \approx P$ the whole rating of the rotorside mains-winding would be utilized. Using a conventional diode-bridge with a chopper the power factor will typically lay around $pf = 0.85$[41], due to commutation inductances. Utilizing power electronics the armature windings can reduce it's ratings with up to 15%. For a thyristor bridge the

pf-considerations are worse since the pf is correlated with the firing-angle. To ba able to provide ceiling voltage of factor 2, the output voltage in steady state has to be kept half the maximum voltage, that is, what voltage that is achievable on the output at $\alpha = 0$. This corresponds to a steady-state firing angle of at least $\alpha = 60°$ and a $pf = 0.5$. In addition comes considerations from the voltage loss due to commutation, increasing the firing angle. The result of this is the mains windings has to be rated twice the size of what was necessary if $pf \approx 1$. In other words, even though the thyristor bridge has a good controllability of u_d, the cost on main windings ratings is quite high compared to the diode bridge.

An alternative to active rectification through a thyristor bridge are Power Factor Correcting (PFC) rectifiers. These can be active or passive and allow for either uni- or bidirectional power flow depending on which topology is chosen. Both buck ($M < 1$)- and boost ($M > 1$) alternatives are available, where the modulation index M is given for boost and buck respectively by;

$$M = \frac{2u_n^1}{U_o}$$
$$M = \frac{I_n^1}{I_o}$$ (29)

The modulation describes the relationship between the AC input and DC-output defining characteristics. A PFC-rectifier has (usually) the following qualities:

- Sinusoidal input currents
- Controlled (to a limit) pf
- Controlled output voltage
- High power density
- Small losses
- Relatively simple topologies and control of these

Sinusoidal input currents are described as $THD < 5\%$ in IEEE-standards[2].
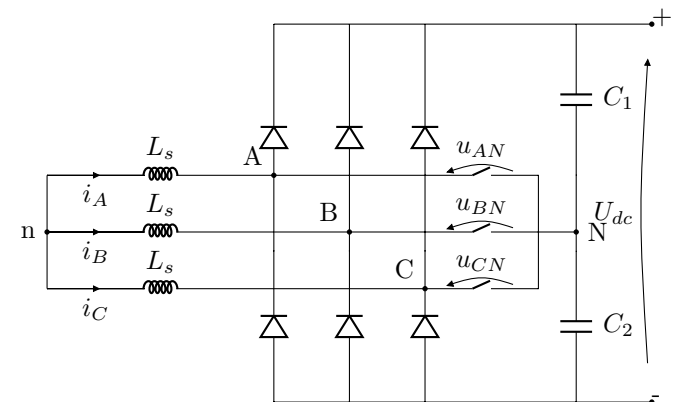
G. The Vienna rectifer

Fig. 16. EC with ideal switches for the Vienna Rectifier

The VR is a boost-type PFC-rectifier which utilizes the capacitators C_1, C_2 to achive sufficient switching-states
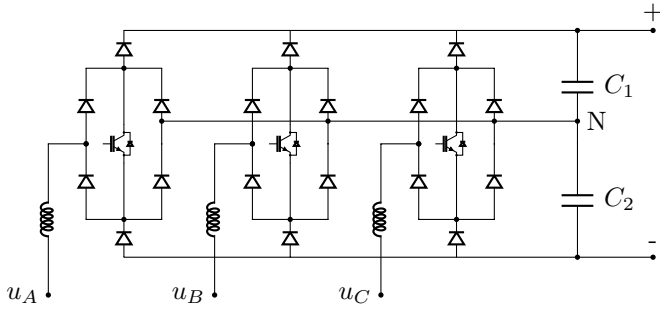
Fig. 17. The Vienna-rectifier realized with many diodes but only three switches.

Fig. 18. The virtual connection illustrates the coupling of phases.

to regulate the output-characteristics and ensure sinusoidal input-currents. The two most common topologies are shown in Fig. 16 where the switches is realized by a pair of antiparallell mosfets or IGBT, and in Fig. 17 the VR is realized with fewer switches but more diodes. For analytical purposes they are the same and Fig. 16 will be used. Defining the voltage-unbalance as;

$$\Delta u_C = U_{C1} - U_{C_2} \tag{30}$$

the voltages u_{Nx} can be written as

$$u_{xN} = \frac{U_d}{2}\left[sgn(i_x) + \frac{\Delta u_C}{U_d}\right](1 - S_x) \approx$$
$$u_{xN} \approx \frac{U_d}{2}\left[sgn(i_x)\right](1 - S_x) \tag{31}$$

The simplification is done considering that Δu_C is keps small to ensure operation of the VR. There is an important requirement (IR) that arises from the topology and eq. (31):

$$sign(u_{xN}) \in (0, sign(i_x)) \tag{32}$$

Considering the system in $\alpha\beta$-coordinates the system can be formulated as:

$$\vec{i_x} = \frac{\vec{u_x} - (u_x\vec{N} + u_N\vec{n})}{\vec{Z}} \tag{33}$$

where $\vec{Z} \approx j\omega L_s$. $u_N\vec{n}$ is the common mode voltage and can be derived assuming an virtual connection $n - N$. This is shown in Fig. 18

$$u_N n = \frac{1}{3}\Sigma u_{xN} \tag{34}$$

From eq. (34) and eq. (33) it is apparent that each phase-switch also affects the current in the other phases and thus are not decoupled.

It is instructive to view the system in $\alpha\beta$-coordinates using the Clarc transform.
From (31) it is apparent that

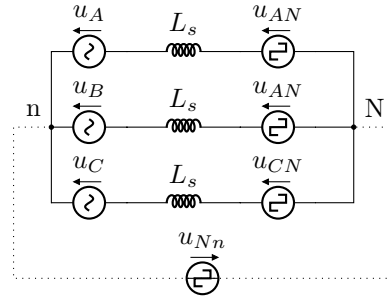$$u_{xN} \in \{\frac{U_d}{2}, -\frac{U_d}{2}, 0\} \tag{35}$$

Eq. (35) generates $3^3 = 27$ possible vectors of $u_{xN}\vec{}$. Subtracting the illegal vectors $u_{xN} = [\frac{U_d}{2}, \frac{U_d}{2}, \frac{U_d}{2}]$ and $u_{xN} = [-\frac{U_d}{2}, -\frac{U_d}{2}, -\frac{U_d}{2}]$ corresponding to impossible combinations of current-signs, leaves 25 possible vectors. Applying the transformation in eq. (2) on these 25 vectors, it results in 19 unique vectors in the $\alpha\beta$-plane. These can be seen as grey vectors in Fig. 19. Theoretically, only four available vectors in the $\alpha\beta$-plane is needed to control the phasor $\underline{u_N}$. In other words, the Vienna rectifier offers a redundancy in switching vectors regarding space vector modulation.
However, due to the IR of the phase-currents there is only $3^2 - 2 = 7$ available vectors at any given time, of which one is the zero-vector $\mathbf{S_0} = [111]$. The available vectors are dependent on the current-polarities. The different combinations are called sectors, and can be seen fully listed in Tab. II.

Sector	$sign(i_a)$	$sign(i_b)$	$sign(i_c)$
1	+	-	-
2	+	+	-
3	-	+	-
4	-	+	+
5	-	-	+
6	+	-	+

TABLE II: Sector-numbering in the Vienna-rectifier

The numbering of the sectors is apparent observing Fig. 19, as they are counted going counter-clockwise. Each sector covers $\frac{\pi}{3}$ electrical degrees. However, the possible voltage vectors in each sector spans $\frac{2\pi}{3}$. Being 6 sectors, they overlap $\frac{\pi}{3}$ degrees. In Fig. 19, the area available to the each sector is shown colored. An important observation is that the different sectors are not sharing all vectors in the shared interval. Sector 1 and 2 is in this example, only share the switching-vector [110] and not [001], which would results in a vector in sector 2 that is a different from the one in sector 1. The IR expressed with sectors can be formulated that $\underline{u_n}$ must be in the same sector as $\underline{i}$.
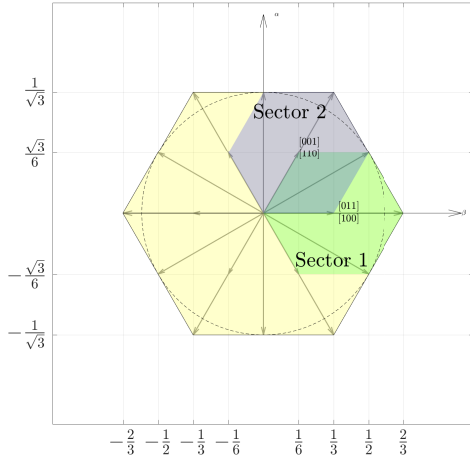
Fig. 19. The possible switching states seen in $\alpha\beta$-coordinates. The numbering og the axis gives the fraction of u_d. That is, the maximum magnitude is $\frac{2u_d}{3}$.
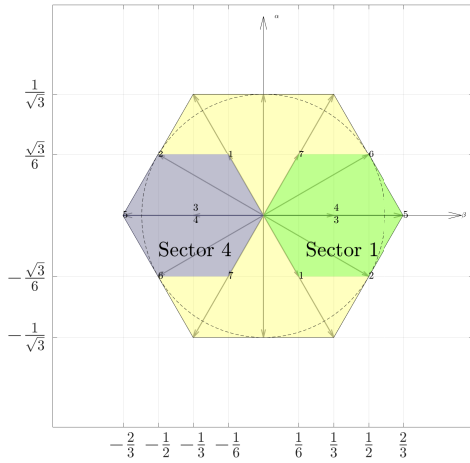

Fig. 20. Due too symmetry the switching vectors can be represented by numbers for better readability.

It is apparent from Fig. 19 that the relative angle and magnitude of the vectors are symmetric across all sectors. In some of the further discussion, the numbering in Fig. 20 will be used. Another key observation which can be drawn from this illustration is the limitation on the modulation index. In connotation with eq. (29) the following should be remembered:

- To prevent collaps of functionality due to unattainable u_n^*: $M < \frac{2}{3}$
- To prevent over-modulation: $M < \frac{2}{\sqrt{3}}$
- To utilize all the neighboring switching vectors: $M > \frac{1}{3}$

These constraints in part governs the design of the inverter and supplying mains. Closer scrutiny of these will be found in the seperate control-chapters.

The charging of the output capacitors by the input-currents is key to the VRs operation. Considering only the DC-link of the rectifier:
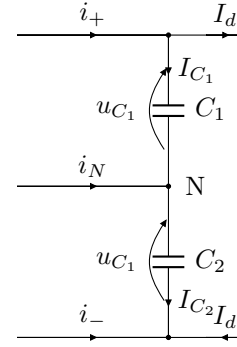

Fig. 21. DC-link only as a basis for the discussion regarding the chargning of the dc-link. Even though I_d follows the shown current-direction, the other will fluctuate and are chosen arbitrarily in this representation.

In connotation with Fig. 21 the following expressions for the current can be found;

$$
\begin{aligned}
i_{\pm} &= \Sigma(1 - S_x)\left(\frac{sgn(i_x) \pm 1}{2}\right) i_x \\
i_N &= \Sigma(S_x i_x) \\
&x \in \{a, b, c\}
\end{aligned}
\tag{36}
$$

Considering the current in the N-node; the following expression can be derived

$$
\begin{aligned}
\frac{du_{C1}}{dt} &= \frac{i_{C_1} - \frac{i_N}{2}}{C} \\
\frac{du_{C2}}{dt} &= \frac{i_{C_1} + \frac{i_N}{2}}{C} \\
\frac{\Delta U_c}{dt} &= \frac{d(u_{C1} - u_{C2})}{dt} = -\frac{i_N}{C}
\end{aligned}
\tag{37}
$$

From (37) it is clear that i_N on average must equal to zero to ensure proper operation of the VR. As a consequence, we can on an average level state that;

$$
\frac{di_x}{dt} \approx \frac{u_{sx} - u_{nx}}{L_s}
\tag{38}
$$

Observing fig.s 20 and 16 it is clear that vector 3 and 4 will have the same qualities regarding producing an voltage $\underline{u_n}$. Using eq. (36) and taking the inverse transformation in 2 regarding these vectors (3 and 4) one sees that these have the opposite effect, switching every second sector. This is summarized in Tab. III. The result is that Δu_c may be controlled independently of $\underline{u_n}$.

$|i_N|$ for the other switching-vectors are summarized in Tab. IV, the sign is sector-dependent. Another results regarding i_N is that it shares the qualities of a zero-sequence current. The reason is as follows: Since u_{Nn} is controlled to be sinusoidal to achive sinusoidal input-currents, one has *on average* a natural point in N that no current should flow into. But this is ofcourse not the case due to switching. A neutral point current in a three-phase

Sector	$\Delta U_C > 0$	$\Delta U_C < 0$
1	100 (**S₃**)	011 (**S₄**)
2	110 (**S₄**)	001 (**S₃**)
3	010 (**S₃**)	101 (**S₄**)
4	011 (**S₄**)	100 (**S₃**)
5	001 (**S₃**)	110 (**S₄**)
6	101 (**S₄**)	010 (**S₃**)

TABLE III: S-vectors which can be utilized for ΔU_C-control

system can be described as a zero-sequence current [42] having harmonics of $f_0 = 3f_s, 9f_s, 15f_s, 23f_s$. This also goes for i_N.

Vector	$|I_N|$
1	Medium
2	Small
3	Large
4	Large
5	0
6	Small
7	Medium

TABLE IV: $|I_N|$ for different vectors

Fig. 22 shows a snapshot of the Vienna in $\alpha\beta$-coordinates where there is a lagging pf at the mains and leading on the input of the VR. Due to the IR (expressed through sectors) there is a limitation on how much $\underline{u_n}$ can lag or lead $\underline{i}$;

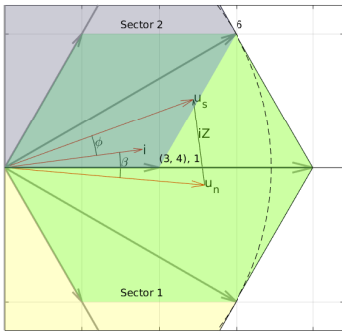$$|\beta| < \frac{\pi}{6} \tag{39}$$

Fig. 22. Current sector is still sector 1. The vector-number in sector 2 is shown in parenthesis, the ones of sector 1 not.

Expressing the relationship in Fig. 22 with phasors;

$$|u_s|e^{j\phi} = |i||Z|e^{j\theta_Z} + |u_N|e^{j\beta}$$
$$\theta_Z = atan(\frac{\omega L_s}{R_s}) \tag{40}$$

It is naturally ϕ that is of greatest interest to us since it is affecting the construction of the mains-windings. The rectifiers input inductance (L_s) draws reactive power. If static power correction is not utilized, this must come from

the rectifier itself. According to this observation it can be seen that the capacitive capacity on the input is larger than the inductive one.

$$|\phi| < \beta \qquad if \quad \beta < 0$$
$$|\phi| < \beta + \zeta \quad if \quad \beta > 0 \tag{41}$$

The constraint of eq. (41) corresponds to leading and lagging current on the input of the rectifier. ζ corresponds to the angle shift due to Z and is dependent both on $|i|$ and Z. β refers to the angle that corresponds to the pf wanted on the terminal of the Vienna. The limitation on power factor in the Vienna is in other words rather strict. A thorough analysis of the role of the input filter and derivation of (41) is found in [24]. The modulation index also effects the flexibility regarding pf at the input of the Vienna-rectifier [16].

IV. IMPLEMENTATION

A. Control

1) Hysteresis-control: In contrast to most of the literature, it is I_f^* which is the governing characteristic in this application, rather than u_d. The concept is as follows: The difference between the reference value i^* and the measured value i result in an error $\epsilon = i^* - i$. It is given that the polarity of $\frac{di}{dt}$ is controllable. To prevent constant switching, there is a tolerance-band, Δh which determines how much from the reference value of the measured value is allowed to fall/rise. If $|\epsilon| > \Delta h$ the polarity of $\frac{di}{dt}$, is reversed so that $|\epsilon|$ is reduced. A general description can be seen in Fig. 23. Note that the upper and lower band can have different distances from i^* in systems where this is needed.
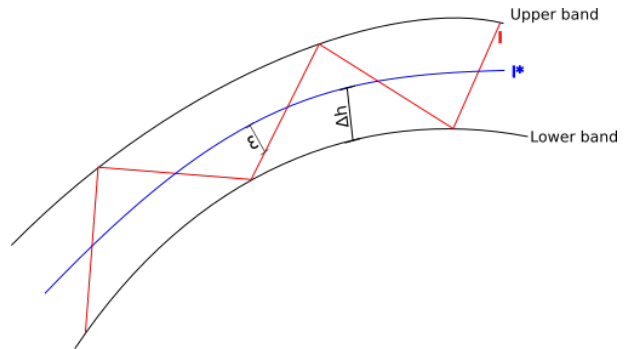

Fig. 23. Controlling i with hysteresis-controll

One of the most mentioned drawbacks of hysteresis-control is the non-constant switching frequency.
Observing Fig. 16, it is apparent that the change in phase currents, $\frac{di_x}{dt}$ is determined both by current polarity and S_x. The magnitude increases if Q_x is closed. This can be formulated as:

$$sgn\left(\frac{di_x}{dt}\right) = [1 + 2(S_x - 1)]\,sgn(i_x) \tag{42}$$

Note that the currents in each phase isn't decoupled in this control-strategy. The magnitude of $\frac{di_x}{dt}$ will be dependent

on the other switching vectors, $S_{\not\sphericalangle}$. Another consequence of eq. (42) is that the polarity of the phase currents has to be gauged to determine the right switching-vector. Equation (42) summarizes to the following switching logic:

$$
\begin{aligned}
s'_x &= \begin{cases} 0 & if\, i_x > i^* + \Delta h \\ 1 & if\, i_x < i^* - \Delta h \end{cases} \\
s_x &= \begin{cases} s'_x & if\, i^*_x > 0 \\ \not{s}'_x & if\, i^*_x < 0 \end{cases}
\end{aligned}
\tag{43}
$$

The methods used to determine i^* will vary between applications and methods. The following approaches have been used in the simulation part of the thesis:

1) Sinusoidal form is a requirement
2) Phase is determined either by PLL or directly from the supply-voltages - if a shift is needed this is calculated relative to it.
3) Amplitude is determined by I_{d*} or U_{d*} through a feedback loop, e.g. PID-regulator. This has proven considerable tuning if an offset isn't used.

Δu_C must be actively controlled to ensure correct operation of the rectifier. This can be done by a second control-loop, adjusting the reference signal depending on Δu_C. The reason for that this very simple control works can be seen from Tab. IV. A larger ΔU_c will cause a higher $|i^*_s|$ and thus less utilization of switching vectors 3, 4, 1, 2 ($|I_N| = large, medium$) relative to 6, 2 ($|I_N| = small$). Seen together with eq. (37) this leads regulation of ΔU_c. The input to this control-loop, easiest implemented as a P-controller, can be Δu_C or the direct cause of Δu_C, which noting eq. (37), is i_N. A conventional hysteresis control which uses a P-controller and Δu_C is shown in Fig. 24.
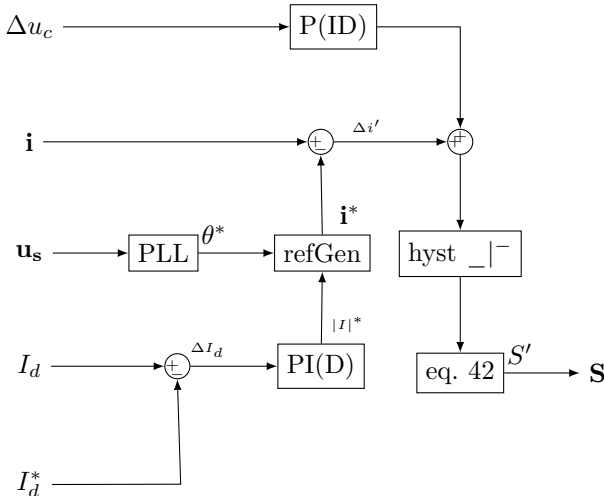

Fig. 24. A very basic hysteresis-control

A more advanced hysteresis control utilizing u_{Nn} and the filter-inductances to decouple the three phases is suggested in [10]. Here, a virtual Nn connection is established like shown in Fig. 18 to calculate the correcting signal to the reference. Yet another control-method that

is used is the injection of a third-harmonic component from i_s into the reference, noting that $f_N = 3f_s$[20]. In addition to a simple and independent control of each phase, this strategy ensures an inherent stability of the center point balance. Moreover, it has also been shown in [25] that it is possible to realize satisfactory current control without use of a controller multipliers. In the scope of Fig. 24, this method is equivalent to greatly simplify the workings of the refGen-box which calculates the actual waveform of the reference current.

B. Control criteria

1) Rough estimation of input-currents: The tuning of the control-loop supplying the amplitude of the input-current is made considerably easier having a set-point which the PID-controller adjust to. In other words, combining a feed-forward model with a feedback loop. Considering a few assumptions one can get satisfactorily results:

- $pf = 1$ at the terminals of the VR
- Lossless operation
- Sinusoidal input-currents and voltages
- A guess estimation $i_{s,guess}$ of the input-current is supplied.

Using the active power on the input and output, as well as the considerations from (40) one can set up the following relations:

$$
\begin{aligned}
P_{out} &= I_f u_f = \frac{I_f^2}{R_f} \\
P_{in} &= \frac{3}{2} \hat{U}_n \hat{I}_n
\end{aligned}
\tag{44}
$$

Equating $P_{out} = P_{in}$, this results in the following estimate

$$
\hat{i_s} \approx \frac{2}{3} \frac{I_f u_f}{\hat{u_n}}
\tag{45}
$$

To determine what magnitude $\hat{U}_{nx}$, one can observe (29) which gives:

$$
\hat{u_n} \in [\frac{1}{3}U_d, \frac{2}{3}U_d]
\tag{46}
$$

keeping the limitation on modulation factor in mind. An mathematical aspect here is that U_{Nn} has been ignored since it *on average* is zero, but in power-considerations over time this still gives satisfactorily results.

In addition to thermal and saturation issues, the VR-lends itself to further constrains on $\hat{i}^*_s$. These are invoked in conjecture with the constrains described below (50) regarding maximum filter inductance. An additional factor limiting $\hat{i}^*_s$ is the zero vector. When the zero-vector is active, no current flows into the dc-link. In other words, $\mathbf{S_0}$ serves to maintain the current form, but in no form uphold the output current. In normal operation this should pose no problems, but this can at higher magnitudes of current limit the operation through the upper limit for $\hat{i}^*_s$.
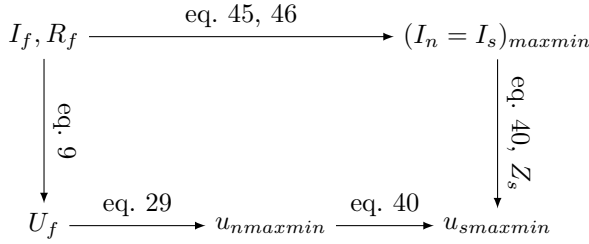
Fig. 25. Flowchart for determining the mains-voltages from I_f and M-limitations.

2) Conflict between capacitor-voltage-difference and current-signal: As $\hat{i}_s$ rises, also I_N must rise due to the operation of the VR. As explained in the theory, ΔU_c also rises and contributes in a to larger degree to the hysteresis-reference. If the current is large enough, this signal will dominate and the current cannot anymore follow it's reference since the capacitor-part is dominating. There exists two solutions to address this issue:

  1) Increase capacitance
  2) Dynamic PID-controller of the ΔU_c

Item (1) is problematic due to realization and size in RPE. Item (2) will only work on very short time scales, e.g. if the reference is set high for a brief moment. If ΔU_c becomes too large the whole operation of the VR is jeopardized.

3) Modulation factor and maximum supply voltage: Designing the Vienna with the hysteresis-control in mind one has to heed the limitation on modulation-factor. Given an mains-impedance Z_s, a field current I_f and the limitation given regarding the modulation factor M. The derivation in the previous subsection is used to determine I_s, but this will not have a large impact as a limiting factor, relatively seen. For typical applications the magnitude of the input-current doesn't need to be found since this will have a small effect on the overall limitation. It is important to emphasize that, given $\hat{u}_s$ from the flowchart 25, I_f may still be increased. The challenges arises if I_f^* falls to minimal values and should be accounted for in the control-strategy. Not doing this would result in the control-strategy trying to achieve an $\underline{u}_n^*$ that lies outside the hexagon of possible switching states shown partly in Fig. 22. This can also be interpeted as a an upper limitation on u_s. Observing the illustration in Fig. 26 it is apparent that a too large u_s results in over-modulation since for the given I_s and Z_s it is not possible to have a u_n inside the hexagon. The size of the hexagon is determined by U_d which again is found from the output current using eq. (11).

4) Minimum field-current: If $\mathbf{S} = [000]$ the VR operates as a diode-bridge and the dc-component of the output voltage is given by:

$$U_{f,000} = \frac{3\sqrt{3}}{\pi}\hat{u}_s \tag{47}$$

The associated I_f can be found through (9). In hysteresis-control the use of individual S-vectors aren't controlled,
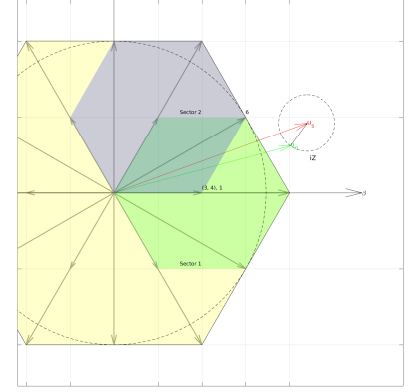

Fig. 26. A too large input-voltage may result in over-modulation.

also not the zero-vector $S_0 = [111]$. This entails that if a $\hat{i}_s^*$ signal is given that is *below* that associated with $i_{f,000}$ there is no way of controlling that the switching-logic produces more instances of $\mathbf{S_0}$ and thus ensuring reduction of i_f relative to $i_{f,111}$. Using the zero-vector and effectively shorting the three phases is the only way of not dumping any current into the dc-link. Baring saturation effects this would also charge the magnetic field in L_s which would result in voltage spikes when the switches changes sign. Therefore,

$$I_{f,min} = I_{f,111} = \frac{3\sqrt{3}}{\pi}\hat{u}_s\frac{1}{R_f} \tag{48}$$

Note that this limitation is only relevant for steady state - during demagnetization a different controlstrategy is used altogether.

5) Winding inductance: Another, crucial limitation of this control-strategy is linked to how fast the input currents may change. Observing eq. (38), this is dependent on three parameters; the supply voltage, the input-inductance and u_{nx}. For the hysteresis-control to work, the $\frac{di_x}{dt}$ must at all times be larger than the rate of change of the reference value i_{sx}^*. This can be put as;

$$\frac{di_x}{dt} = \frac{1}{L_s}|(u_{sx} - u_{nx})| >> \frac{di_x^*}{dt}$$
$$\frac{di_a}{dt} = \frac{1}{L_s}|(U_{sa}\sin((\omega_s t) - u_{na})| >> \hat{I_a}^*\omega\cos(\omega_s t) \tag{49}$$

Here phase A is used to and defined with no shift from a sine wave for illustration purposes. In the hysteresis-scheme the different switching strategies are determined independently and thus the "worst case" should be considered. These can be summarized as:

  • $\sin(\omega_s t) \approx 0$
  • $i_s = \hat{I}_s$, may be found from eq. (45)
  • $u_{nx}^- = \frac{U_d}{3}$, observing eq. (46)

Rearranging eq. (49) for L_s and considering the worst case situation, the expression becomes:

$$L_s << \frac{I_f R_f / 2}{\omega_s \hat{I}_s} \qquad (50)$$

As the simulations will suggest, L_s should be as small as 20% of the maximum inductance found in (50). This is due to the fact that also the other phases will be affected by faulty switching.

Traditionally, the input impedances is calculated from a minimum value since common applications haven't been to connect the VR to windings with such stator inductances as in the case with RPE. To smooth the current than a minimum inductance need to be calculated. This minimum inductances can be found from:

$$L_s > \frac{u_s - u_n}{\Delta I_s f_\Delta}. \qquad (51)$$

Equation (51) can't give an unambiguous result alone since u_s varies through the period while u_n according to (35) is semi-constant. Using PWM-control f_Δ is constant, but in the case of hysteresis-control this will wary. The average switching frequency is not easily determined since it is also determined of the system and thus also L_s and ΔI_s. A upper limitation on f_Δ may be set to minimize switching losses and ensure correct operations of the drivers.

6) Additional chopper: Due to the large time constant of the field-winding, there should be implemented some kind of additional circuitry to possibly hurry the demagnetization. A simple and effective topology is to use a single-quadrant chopper. This will be connected on the output of the VR. Utilizing this chopper one may also greatly simplify the control of the VR. In this control-scheme the VR only controls the total voltage of the DC-link and ensures sinusoidal input-currents. The chopper ,using pwm or hysteresis-control, controls the output current. The addition is shown in Fig. 27.
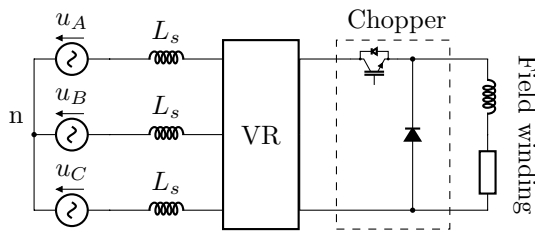

Fig. 27. The addition of a chopper makes faster demagnetization possible.

The chopper decouples the amplitude of the input and output currents. This makes an important control-constraints of the hysteresis-control void, namely eq. 48 setting a minimal I_f. What $\hat{i}_s^*$ goes, this could now be derived from the desired U_d. U_d^* should be set at least to:

$$U_{d,absmin}^* >> 2U_f^* \qquad (52)$$

This is motivated that in the case of a need to go to ceiling-voltages (2 p.u.) this could be achieved by changing the on-times (possible turning completely on).

7) Communication: In the case of brushless excitation with an active rectifier an communication link needs to be used. There is a wide variety of RF-transmitters in the marked several protocols (Wi-Fi, Bluetooth, Ziigbee etc.) that has been applied in wireless control of power electronics. Nonetheless, one has to make the consideration regarding switching-frequency and baudrate of the communication link. For switching of e.g. IGBTs in the circuit the necessary transfer-frequency is:

$$f_t \approx f_p(RN_Q + K) \qquad (53)$$

where f_t is the transfer rate, f_p is the switching rate, R is the gross bitsize of each turn on/off signal, N_Q is the number of devices that needs to be switched and K denomenates the number of bits that needs to be transfered regardless of number of switching devices, e.g. the Start and Stop byte in the I^2C-protocol. Alternatively one also puts the PLS on the rotor together with the power-electronics. In this case, it is measurements such as stator-voltage that needs to be transfered over the air gap.

Example VR with rotating PLS:

PLS	Stator $\rightarrow$ rotor	Rotor $\rightarrow$ stator	f_t
Stationary	Q_1, Q_2, Q_3	$U_{C_{1,2}}, i_f$	$400|400 kbit/s$
Rotary	u_{stator}	NA	$240|0 kbit/s$

TABLE V: Examples of necessary transmission-frequencies, K = 2 byte, R = 1 byte, $f_p = 10kHz$, size measurement = 1 byte (signed)

These numbers are obvious only crude calculation seeing that protocol and leeway for biterrors must be taken into considerations. The aforementioned communication protocols bitrates can be seen in table VI

Protocoll	Bitrate	Frequency	Non-overlapping channels
Zigbee	20-250 kb/s	2.4, 5 GHz	16
Wifi	11-54 Mbits/s	2.4, 5 GHz	3, 24
Bluetooth	24 Mbits/s	2,4 GHz	79

TABLE VI: Qualities of different wireless technologies[3].

There is also possibile to utilize different channels for different devices, drastically reducing the need for transferring-speed down to possible f_p. This may however increase the challenges setting up the system. In the case of Bluetooth this could also lead to interference since it uses channel-hopping as strategy for non-inteference. With only a few different signals utilizing Bluetooth this should pose no issue, but should be heeded if one uses many devices[53]. Seeing the tables V and VI it is obvious that there is quite much leeway regarding transfer speed with todays wireless technology.

RF-communication can however be disturbed by the EMI-noise in the machine due to power electronics and

stray magnetism. In [50] an infrared communication-link were designed and successfully deployed in an asyncronous motor-set up where traditional telemetry would not work.

C. Capacitors

Capacitors come in a wide array of sizes, construction and material. In power electronics there are mainly three main types that may be considered[9];

(a) Metalized Capacitors
(b) Film/foil capacitors
(c) Hybrid capacitors

Whilst (b) normally are designed for high $\frac{dv}{dt}$, but has a lower power density and lacks the self healing capability of (a). The self healing - capability entails that a point break-down of the dielectric material will be automatically cleared at the cost of a minimal reduction of capacitance. (c) combines the technology of the two former types. The incentive for minimizing volume and ensure long, undisturbed operation favours (a), but due to better $\frac{dv}{dt}$-characteristics (b) may still be the best choice since a high $\frac{dv}{dt}$ is experienced in conjunction with certain demagnetization strategies.

1) Voltage rating and voltage ripple: Following the same philosophy as in eq. (37) and Fig. 21 an expression describing the voltage-ripple can be formulated as:

$$\Delta U_d = \frac{i_+ + i_- - 2I_f}{C} \frac{1}{f_\Delta} \tag{54}$$

Since both f_Δ and the magnitude of i_+, i_- will wary through a period for the VR, eq. (54) can't be used for direct sizing of the output capacitors. But qualitatively it shows that the output capacitors have to be scaled proportional with I_f and inversely with f_Δ which is reduced by reducing the hysteresis band. As mentioned it is i_f rather than small variations in u_f that is of relevance for this application, and in most cases it is rather the ΔU_c limitations rather than ΔU_d that determines the minimum size of the capacitor. Using eq. (37) and only considering the fundamental of i_M with frequency $3f_s$, the expression can be roughly formulated as

$$\Delta U_C = -\frac{1}{C} \int_0^\pi \hat{I}_M^1 sin(3\omega_s t) dt \tag{55}$$

The limits is taken as $[0, \pi]$ since it is this half-period that is used for one charging/discharging of a capacitor. Solving the integral and rearranging for C gives:

$$C = \frac{2\hat{I}_m}{\Delta U_{c,max} 3\omega_s} \tag{56}$$

The rms-value of I_m can be found using eq. (58) and ΔU_c should be held quite small regardless of lack of influence on the magnetic field. This is due to fluctuations in u_D will cause the octagon in Fig. 20 to pulsate. If M is close to the upper limit of $\frac{2}{3}$ then this may cause periodical over modulation.
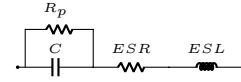

Fig. 28. The EC of a real capacitor. R_p consist of leakage and insulation resistance.

2) Ripple current: A real capacitor can be described with ideal components in circuit in Fig. 28.

ESR and ESL denotes Equivalent Series Resistance and Equivalent Series Inductance. Of the parameters in Fig. 28, only ESR is key for the dimensioning of the capacitors since the power dissipated is:

$$P = I^2 ESR \tag{57}$$

Power dissipation reduces the capacitor life time and contributes to the heat-production of the circuit [13]. ESR is increasing with an increase in temperature, but for relevant frequencies $f_M = 3f_s << 10kHz$ it is held constant[9]. Considering Fig. 17, the rms-current through each capacitor is split equally to ensure $\Delta U_c \approx 0$. Considering Fig. 22 and eq. (29) it is clear that the larger $|i_N|$ is, the larger also the modulation index M is. Buy calculating the fraction of total switching time each state has and seeing this in connotation with what i_M is in each switching-state is, integrating over one symmetrical period ($\frac{2\pi}{6}$ since $f_M = 3f_s$) an expression for the rms-current in the midpoint were found in [21];

$$I_{M,rms} = \sqrt{\frac{5}{2}\frac{\sqrt{3}M}{\pi} - \frac{9M^2}{4}} \hat{I}_n^1 \tag{58}$$

[21] also provides an analysis of the midpoint current and other relevant qualities of the topologies under unsymmetrical loading of the VRs input. The midpoint rms-current must be evenly split between C_1 and C_2 to maintain voltage balance, thus;

$$I_{C,rms} = \frac{I_{M,rms}}{2} \tag{59}$$

which in connotation with (58) is a dimensioning eq. for the output capacitors regarding heating.

D. Thermal considerations

In an applications that not strictly is meant for demonstration, cooling of IGBT modules are necessary. Due to the strong forces convection the RPE would experience from the rotation the cooling rigs should be possible to make smaller then the ones implemented in commercial products. Due to the limited scope of this thesis this issue is not considered here.

1) Trace-width and thickness: There are several suppliers that offers cheap PCB-printing, usually for copper layers at $1 - 3oz/ft^2$. For gate-signal and readings this is of no further concern, but for the current carrying parts of the topology heat development as a consequence of I^2R-losses may become a significant high. Both width and

thickness contributes to the track-resistance. According to IPCs standards [19] the rms-current capacity is given by:

$$I = 0,048DT^{0,44}(Wi \cdot Th)^{0,725} \tag{60}$$

where DT is temperature rise in C°, Wi is the track width and Th is the track thickness both in mil $(1-3$ inch). The power-dissipation of the circuitry as such arises mainly from the switches and the diodes as shown in section **??**, so the relevance is primarily for the dialectic of the PCB. Even thought FR4-graded material often used in PCBs are rated to $130C^\circ$, DT should be kept way lower to not waste power or affecting components. If no realistic combination of trace, DT and current can be found, one should revert to using soldered wires.[5].

E. Case - testrig Svante

The inspiration for this thesis comes from previous work[29] using this testrig and these dimensions will be used as initial parameters in the simulations of the different aspects of the VR as excitation topology.

1) Electrical parameters:

I_f*	$50A$
U_f	$150V$
R_f	3Ω
L_f	$2,96H$
$\hat{U}_{s,LL}$	$125V$
f_s	$50Hz$
R_{ph}	0.2Ω
L_q	$2,720mH$
L_d	$2,650mH$
L_s	$2,685mH$
C_{link}	$3,3mF$

TABLE VII: Same parameters as used in [30]. L_s is taken as the mean of L_q and L_d.

2) Possibility for re-connecting main windings: Each phase of the supply windings consist of two windings shown in 29 which can be connected either in series. In the parameters given in table VII, they were connected in series.
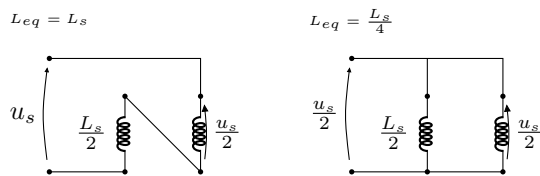

Fig. 29. Connecting the split-windings in series (left) and parallel (right) have consequences for the inductance and the voltage.

As shown in Fig. 29 the voltage and inductance *of each winding* stays the same between the connections, but the output of each winding that feeds the VR will be different.
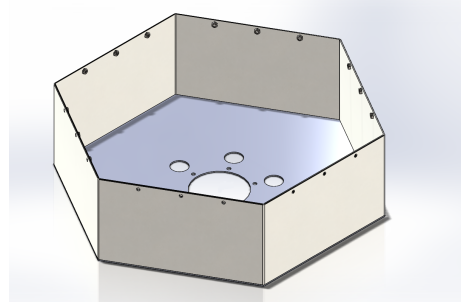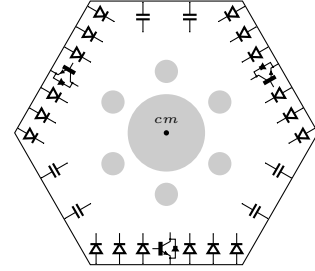

Fig. 30. The box containing the RPE

Fig. 31. Note that the drill-holes are not to scale.

3) Enclosure for RPE: For earlier research a mounting box has been build to house the RPE, of which a CAD-drawing can be seen in Fig. 30 and a simplified overview in Fig. 31.

To avoid oscillations and unequal distributed stress on the box itself the components should be distributed in such a manner that the center of mass (cm) is in the center of Fig. 31. Only the current-carrying components are shown since they naturally have to be significantly larger then the gate-drivers and such. To simplify design three identical boards with the same components be used, each consisting of one leg of the inverter. This is shown in Fig. 31 by indicating which component goes on each side. To ensure balance in the box C_1, C_2 must be realized by connecting several capacitors which sum is multiples of 3. Here the minimum number of capacitors is shown. Due too availability of large (mF-scale) film-capacitors it would probably be necessary to connect several capacitors in series anyway to achieve the desired capacitance. To further simplify the design of the boards, the six (or more) capacitors could be distributed on the same sides as the legs. Thus it will be need for a single layout and mechanism for securing the boards to the sides of the box.

F. Overview

The sizing of the components in the Vienna can be summarized in the flowchart shown in Fig. 32. In all steps simulations should be conducted, the analytical expressions is in some cases approximations that only serve as an initial suggestion. As far as it is possible, L_s and C should be adjusted rather than L_f since this involves considerable more work and challenges regarding

the mechanical issue. The motivation for increasing L_f is to produce the same flux with a lower current and thus different ratings for the exciter (ref. eq. (10)). This adjustment must be noted is strongly governed by the mechanical constraints on the rotor since space is limited and thus also the number of windings and length of solenoid making up the winding. Noting eq. (17), increasing the number of windings would increase the resistance and thus u_f. In the scope of the VR this is actual beneficial since in lends greater flexibility regarding u_s and L_s. This can be seen following the flowchart in 25 and considering eq. (46). In addition to suffer from strict mechanical constraints, to change the windings of the rotorwinding is a considerable endeavor. It is mentioned here mainly as a possibility to illustrate the effect the rotor-winding inductance has, and thus shown with stipled lines.

In most exciter the same would go for N_s, but as explained it is an easy task to reduce the *effective* windings by switching from series to parallel connections. But still, in this case only two modes are possible. Furthermore, in most applications the VR are meant to be fitted to an already constructed exciter and generator. In this case N_s, L_f is given and one has two less degrees of freedom in the sizing of the VR. When the question "Mechanical viable" is asked, this is regarding space on the rotor for the power electronics, cooling and the winding. In this flowchart it is given, but this is possible to increase with different box-design. Static compensation in the case of $Ls > L_{s,max}$ due to pf-limitations of the Vienna is not described here.
Also, the generator-specs will affect more steps than is directly shown here. $\omega_{s,mec}$, N_{stator}, Ψ_s unsoforth will effect the dimensioning cooling system (utilizing forced convection), the mains-supply windings, the field winding and the mechanical leeway for the RPE.
From eq. (50) reducing ω_s may seem as an viable alternative for increasing the maximum limit of L_s and thus avoiding the issues that entails with to great winding-inductance. The induced voltage to the feeder is proportional to ω_s since $\frac{dA}{dt}$ in eq. (18) is a consequence of ω_s. Reduced voltage at the mains would warrant higher $\hat{i}_s$ to deliver the same power to the VR and according to eq. (50) the effect of lower ω_s would cancel out. If increasing Ψ_s were an option however through e.g. increasing the magnetizing current on the stator, ω_s could be reduced and keep u_s and thus i_s constant by increasing Ψ_s. This is not a case with PM-excited supply-windings since the magnetic field from the stator side is constant.
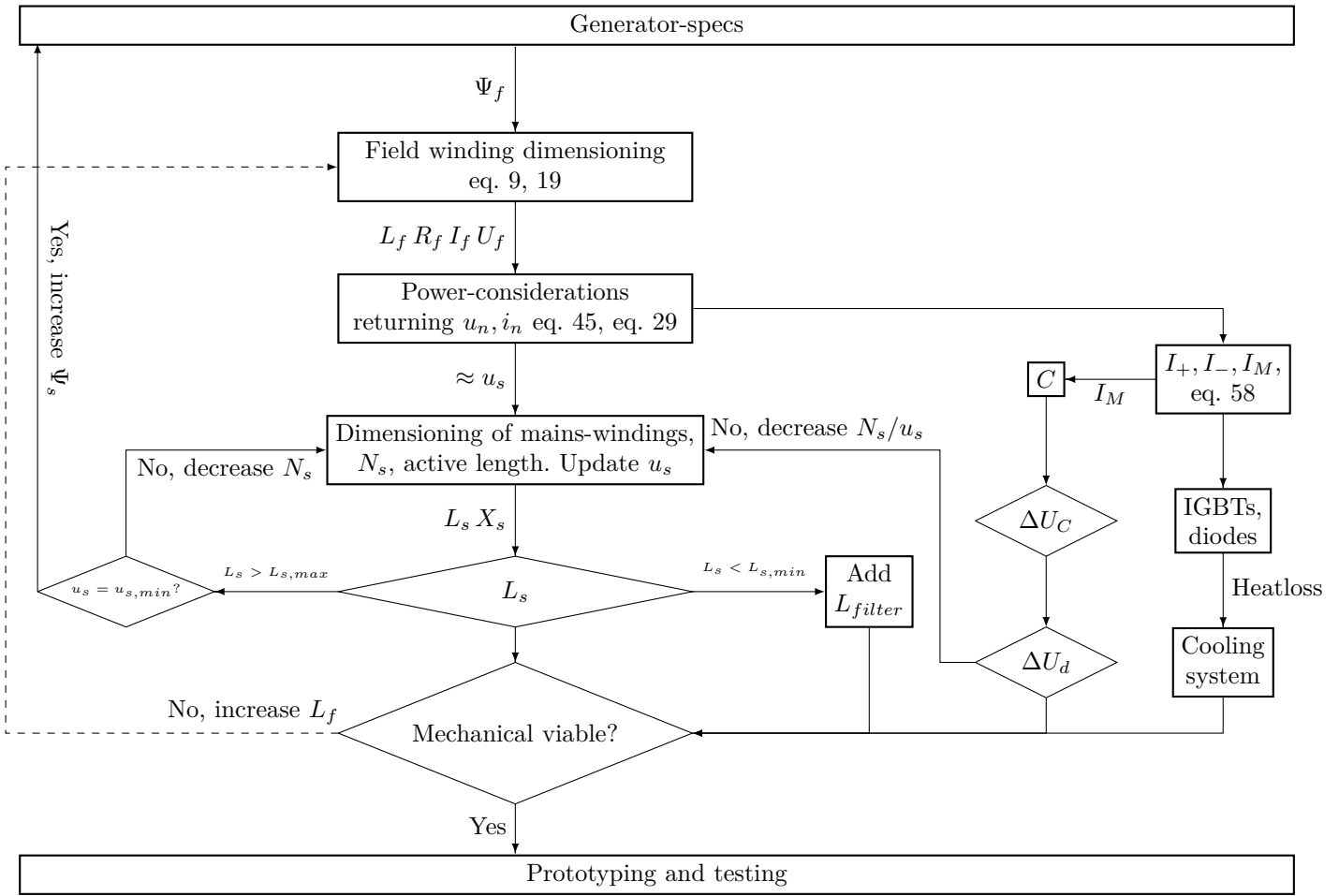
Fig. 32. A selective overview of the approach designing a VR for the excitation purposes.

V. SIMULATION RESULTS

The simulations were conducted using the Matlab Simulink add-on Simscape Power Systems. Only the Svante-case will be discussed here, but the same model were used to verify the building of the demonstration-circuitry. The three-switch version of the VR shown in figure 17 is used. For control purposes the simple hysteresis-control described in the control-chapter were applied. In simulations of the demagnetization techniques the same models were used, but after the demagnetization signal was given a different switching strategy were deployed.

A. Steady state

1) Initial calculations: In sections III-G limitations regarding the supply voltage U_s and L_s were given. Applying these calculations on the parameters given in table VII the following were found;

- $\hat{U}_{sLL,max} = 190V > 125V$
- $\frac{L_{s,\ ABSmin}}{L_s} = 1.13$

As shown above, the parameters cause no issues regarding the constraints on supply voltage. The large field-winding inductance will however cause some problems using the hysteresis-control. The effect of NOT heeding this limitation is shown in Fig. 33.
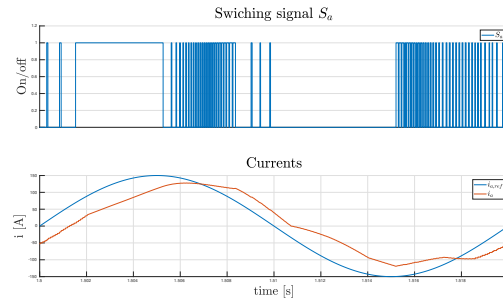
Fig. 33. Clearly the actual current can't reach the reference value. The reason for the pulses are the result of the ΔU_c-regulation and the limited period when the current are inside the hysteresis-band.

There is three possible solutions to this problem:

1) Adopt more complex control strategies, e.g. PWM-control
2) Reduce L_s
3) Review model and other parameters

Using the PWM-control will again possibly meet other

pf	$THD_{ph,V}$	$THD_{ph,I}$
0,98	0.66	0.04

TABLE VIII: Measures of power quality on the input for the instant when $i_f = 50A$. Note the high THD on for the input-voltages.

challenges described in [16]. This alternative will not be considered here. Reducing L_s through fewer windings as a possibility is described in section III-B4, but as mentioned there this entails some other challenges so this alternative was not analyzed in the simulations. Two other alternatives, shown in three different models shows however solutions to the problems. These will be shown in the following and are:

- Changing the main windings connection
- Using wound exciter
  - Emulating a wound exciter using the Simulink modell for a synchronous machine
  - Considering only the transient reactance in conjecture with ideal voltage sources.

B. Changing main windings connection

Considering the possibility of changing the windings connections shown in Fig. 29, there is still a possibility for the VR to be tested in the Svante testrig "as it is" without exchanging the PM feeder with a wound one. With the new values (note that also $R'_s = \frac{R_s}{4}$), the initial calculations regarding the controllability criteria gives:

- $\hat{U}_{sLL,max} = 86V > 65V$
- $\frac{L_{s,\ ABSmin}}{L_s} = 0.27$

The initial simulations of the model with these changes in parameters may be seen in Fig. 34.
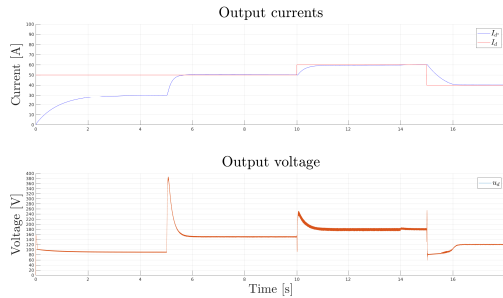
Fig. 34. The VR starts to act at $t = 5s$. At $t = 10s$ is I_f* raised 20% to $I_f = 60A$, and lowered 20% to $40A$ from the original after another 5 seconds.

The current waveforms from the three phases can be seen in Fig. 35.

It is clear that the problems with following the reference current is increasing with $\hat{I}_s$ as suspected. However, the current can still be considered sinusoidal.

The power-quality measurements can be seen in Fig. 83, and the results thereof can be seen in Tab. VIII.

Central to the VRs operation is the stability of ΔU_C, described by eq. (37). A snapshot of these two qualities in the simulation can be seen in Fig. 36.
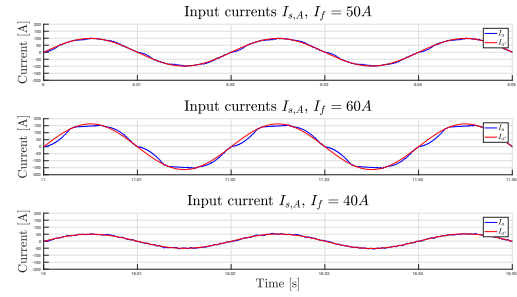

Fig. 35. The effect that the output currents have on the inputcurrents are obvious. The distortions around the zero-crossings are more pronounced the larger the output-current (and thus also the input currents), are.
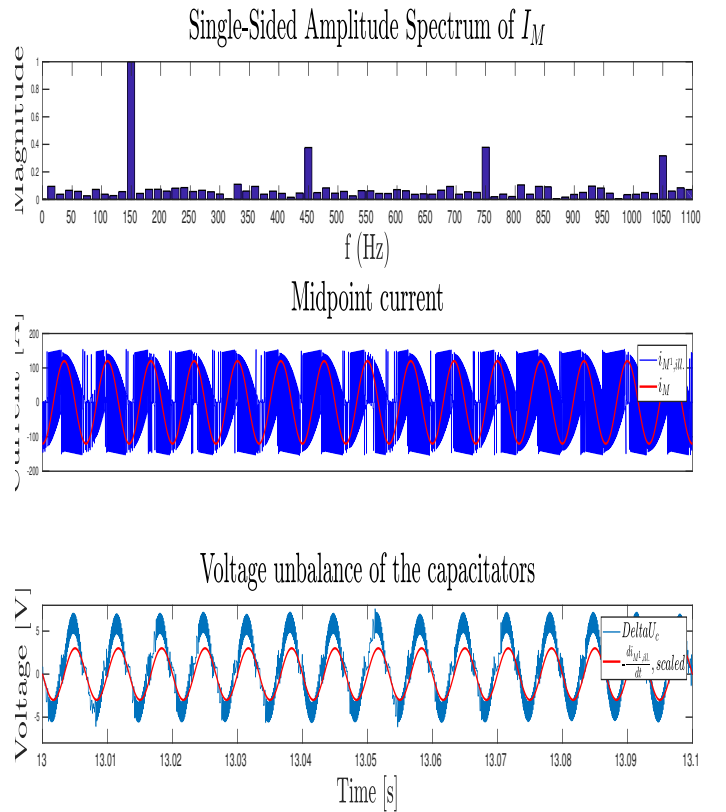

Fig. 36. In the upper plot, the frequency-spectrum of the middle point current is shown. Frequency-wise the results is as expected with $f = 3f_s, 9f_s, 15f_s...$. As an illustration, a sine signal is superimposed in the plot of the middle point current in the middle plot. This makes the results from the frequency-spectrum easier to see. In conjecture with the lower plot, showing the fluctuation in the difference in output-capacitor voltage, this confirms eq. (37). The derivative of the middle point current increases and decreases ΔU_c. The frequency-analysis were done with the power_fftscope-package of Matlab.

These results shows that the control works and that the VR is a viable option for testing at the Svante Testrig if the necessary re-connections were done. The currents

are as good as sinusoidal and the pf on the input is quite satisfactory. The high THD of the voltages on the input is due to the switching. In contrast to PWM-control, the hysteresis-control isn't focused on ensuring sinusoidal voltages on the input of the VR and thus also sinusoidal currents.

1) Machine-model: The actual three phase windings beeing induced with voltage u_s will have a different behavior than an ideal voltage source with an inductance in several respects. The main difference in this problem is that the reluctance of the stator-windings will be described thought the synchronous, sub-transient and transient reluctances. The exciter in Svante testrig earlier used are using PMs and $X \approx X' \approx X''$. Using this exciter to achieve good operation with the hysteresis controlled VR, one can expect problems as shown in the initial calculations. However, using a wound exciter there typical is a great variation in the reluctances. The derivation of this relationship is thoroughly shown with typical values in [23]. The values chosen are found in Tab. IX. To simulate this case, the Simulink PowerSystems Synchronous Generator p.u. model were used. To closer resemble the situation in the Svante testrig some modifications were done, namely;

- Change number of pole pairs and frequency to give an output frequency of $f_s = 50Hz$
- Set a constant field-winding voltage that in no-load conditions delivers $U_s = 125V$
- $R_s = 0.2\Omega$
- Rather than using an L_s, the stator winding is shown in Tab. IX.

X	X'	X''
1.5	0.3	0.2

TABLE IX: Stator reluctances. A round rotor is chosen and the simplification $X_d \approx= X_q = X$ is applied, values in p.u.

Implementing a non-grid/mechanical element poses another challenge regarding creating the reference i_s^*. Due to switching the terminal voltages of the feeder will not be sinusoidal and not possible to use as a reference-form for i_s. Two possible solution to this challenge are:

- Using fundamental of u_s found through Fast Fourier Transform
- Using rotor-angle

The second option were used in this case. In a real-life application this warrants absolute position sensors on the rotor, but this is in many applications already implemented and does not pose any large challenge for the relatively slow hydro generators which this excitation system is intended for. The computational effort is also greatly reduced. The reference generator from the rotor-angle is shown in Fig. 81. The measured stator voltages and the reference waveform (scaled) can be seen in Fig. 37 which indicates why the rotor-angle can be used to determine a fundamental for control-purposes:
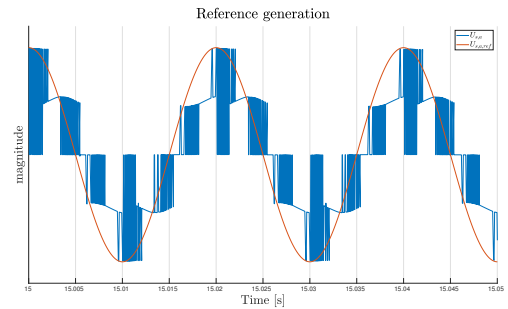

Fig. 37. Even thought the measured stator-voltages are erratic, the fundamental shows a clean sine-wave-form. The small shift is due to that the load-angle isn't taken into account here. To compensate for this, a shift in the reference may be inserted in the control to ensure $pf = 1$.

Utilizing the mechanical feeder shown in Fig. 82 results in a smoother current-form and closer to the reference as shown in Fig. 38, relative to the initial simulations.
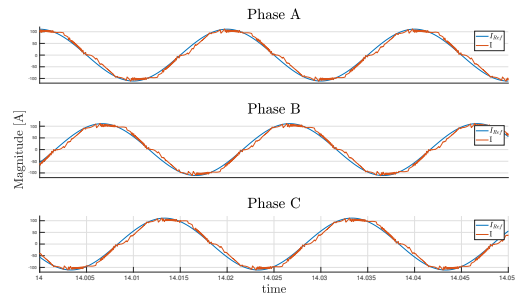

Fig. 38. Three phases interfearing with each other

Still, it is obvious that the currents has trouble following the reference-currents around the zero-crossing. This is in compliance with the derived eq. (49) where it is stated that it is close to $\omega t = 0$ that the control-criteria regarding $\frac{di_x}{dt}$ is the most critical. Each time one phase falls out of the reference-boundaries, the two naturally are affected since the system is a star-connected. This is also apparent from Fig. 38. Rather than adjust the parameters further, this "fault" will be carried on with the further simulation. The reason is that the THD and pf is of such good quality that this distortion is manageable. Due to lack of knowledge and the considerable simulation time of the model making the use of "trial and error"-method time consuming, a constant to the the $\hat{i}_s$ were implemented. This made the choice of the PID-parameters easier to get the desired result. The offset were calculated using the approximation in eq. (45). Since U_s isn't a given parameter in the generator, the no-load terminal voltages of the generator were used. The calculation of the amplitude $\hat{i}_s^*$ can be shown in Fig. 84. The operation where the Vienna reaches steady state is shown in Fig. 39–

A rapid step in i_d^*, will cause a large increase in $|i_s^*|$, only limited by the reactances of the machine supplying the VR. The VR will without further control or circuitry for a short moment cause a short of the three phases.
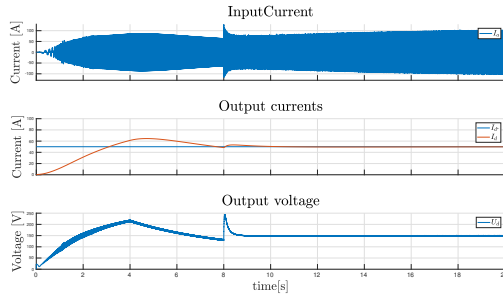
Fig. 39. From $t = 0$ to $t = 4$ the speed of the machine follows a ramp up to steady state speed. At $t = 8$ the Vienna starts to operate. Although not very clear from this plot, the increase in the amplitude of the inputcurrent is due to $i_d < I_d*$ after the initial overshoot. This adjustment is slow, unlike the step that is experienced at $t = 8$.

This is apparent from the switching-logic of the hysteresis-control. Considering the model in Fig. 16, the voltage over L_s becomes $\frac{u_{s,LL}}{2}$. This causes the magnetic field stored in the inductance momentarily to increase. Later, when normal operation is resumed due to satisfactory increase in input-current, this magnetic energy is dumped into the capacitors since the inductive load doesn't allow for a rapid current change. This is the cause for the voltage spike shown in Fig. 40. In combination with increased i_s^*, this results in a step in i_f. In Fig. 41 the switching-logic in action during the step and the following consequence for the current is shown.
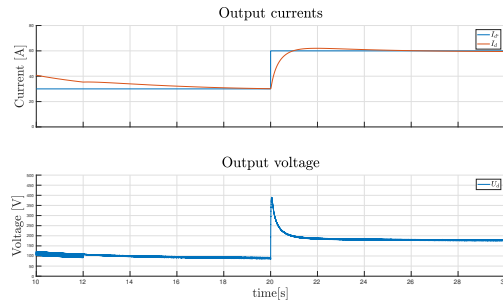
Fig. 40. At $t = 20$ a step $i_f*' = 2i_f*$ is given. The subsequent voltage and current rises are shown.
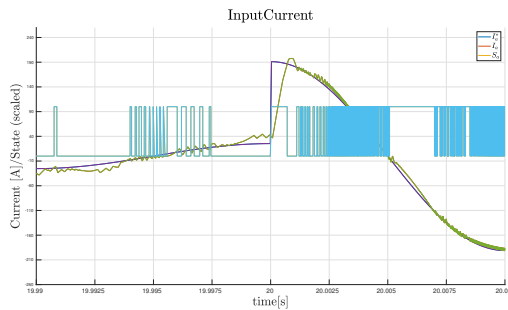
Fig. 41. L_s limits how rapid the current rises.

2) Simplified model considering only X": To simplify simulation and analysis, the model shown in 80 will be used for the further discussion. As shown in the initial calculation and simulation, the parameters of the Svante-exciter is not suitable for a VR with hysteresis-control. Furthermore an wound feeder is modeled, and u_s is taken as a variable that can be calculated. The new parameters can be seen in Tab. V-B2

I_f*	$50A$
U_f	$150V$
R_f	3Ω
L_f	$2,96H$
$U_{s,LL}$	$90V$
f_s	$50Hz$
R_{ph}	0.144Ω
L_s	$0,36mH$
C	$1,5mF$

TABLE X: The new paramenters

L_s is estimated by taking $L_s = 0.2L_{s,old}\sqrt{\frac{u_s}{u_{s,old}}}$. The factor of 0.2 is because only X'' is considered and the scaling with the square of the voltage is due to the need for fewer windings. U_s is taken as the largest value that satisfied eq. (48). With these parameters $i_{f,nom}$ starts of the lower part of the possible range, enabling the simulation to illustrate a step in reference. At $t = 5$ the
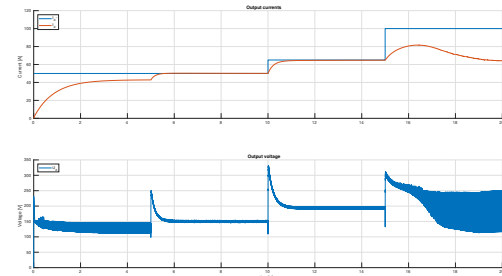

Fig. 42. Illustration of stepping and reference finding.

VR is turned on and adjusts to $i_{f,5} = 50A$. At $t = 10$ a step in the of 50% is given. The actual value doesn't quite reach the reference due to lack of PID-tuning and short adjustment time. At $t = 15$ the reference is given higher than the VR can handle and the operation breaks down. This indicates that the VR may deliver ceiling and current of $1.5p.u.$, but not the demands of $2p.u.$. The reason for the breakdown is that $i_s^* > i_{s,max}^*$ as described in the control-chapter. As can be seen from Fig. 43, which illustrates the situation before and after breakdown, the usage of $\mathbf{S_0}$ increases and results in no increase in the energy delivered to the field-winding despite higher input-currents.

In Fig. 43 $d_{S_0} \approx 50\%$. In other words, half the current that goes into the VR is just used to maintain current form and doesn't deliver any power to the rectifier. Since the output-current doesn't rises, the control-algorithm reacts by increasing $\hat{i}_s^*$, worsening the problem and breaking the operation. In a real implementation it is necessary to implement a saturation-function to ensure that $\hat{i}_s^*$
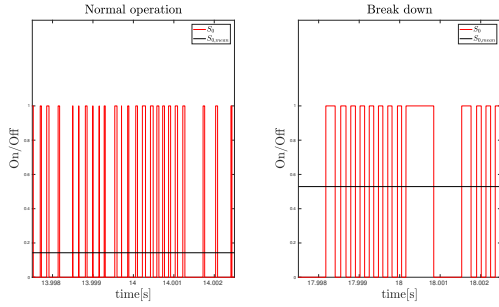
Fig. 43. Wheter or not $\mathbf{S_0}$ is active is shown in these plots along with the average duty-cycle of this situation.

doesn't rises above $i_s, \hat{max}^*$. Here it is shown merely as an illustration. An alternative solution is to design a control strategy that tracks the use of the $\mathbf{S_0}$-vector and acts accordingly to avoid over-usage and thus possibly reaching $2i_{f,nom}$. This would be rather counter-productive since the whole point of using hysteresis-control is it's simplicity.

As mentioned in the theory-chapter, is the regulation of the current-waveform and ΔU_c working against each other, however on different time-scales. The consequence of not adjusting these two parameters in conjecture is shown in Fig. 44. $K_{p,\Delta U_c}$ is initially set rather large, before it is set to a more suitable value at $t = 14s$
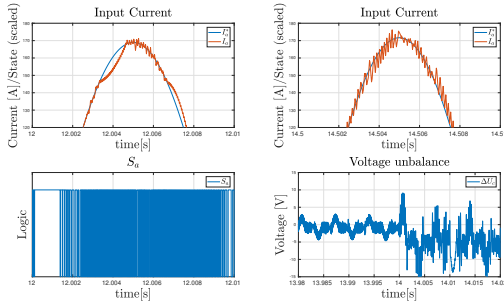
Fig. 44. NW shows the distorted current waveform due to a large $K_{p,\Delta}$. SW shows the corresponding switching signal, S_a. In NE $K_{p,\Delta}$ has been reduced. SE shows the consequence for ΔU_C of reducing $K_{p,\Delta}$.

The behavior in the SW part of Fig. 44 seems at first puzzling - since $i_s^* > i_s$ for a longer stretch, why are S still switching? The reason is the input from the ΔU_c into the hysteresis-control. This is now so large that it overrides the signal ensuring a smooth waveform. This is no longer a problem in NE since $K_{p,\Delta}$ has been reduced. However, this is done at a cost, namely a larger ΔU_c. This can be seen in the SE part of Fig. 44 where ΔU_c rises almost immediately after a change in the P-parameter.

3) Adding chopper: Introducing the chopper changes the controls in two respects

- The chopper governs I_f
- The VR governs the voltage of the output DC-link

The control-parameters for the chopper can be seen in Tab. XI. The implementation in Simulink is shown in Fig.

86. The input into the PID governing the amplitude of the input current also changes. Before the input was ϵ_{I_d}, now it becomes $\epsilon_{U_d} = U_d - U_d^*$. U_d^* is set to be $2i_f^*/R_f$ to ensure that the chopper has sufficient voltage from the dc-link to conduct suitable switching also after the necessary step of $i_f^{*'} = 2i_f^*$

f_{PWM}	$5kHz$
$K_{p,PWM}, K_{i,PWM}$	$3, 0.2$
ΔI_f	$0.4A$
R_{demag}	$10R_f$

TABLE XI: Parameters for the two different controls for the output-chopper.

This enables a much lower output current, and thus a larger range and possibility to achieve a step of $i_f \rightarrow 2i_{f,nom}$. A demonstration using the same parameters as earlier, but with $i_{f,0} = 40A$ is shown in Fig. 45.
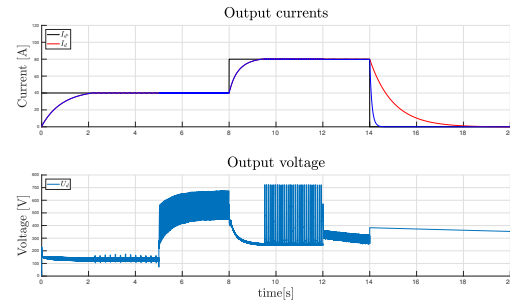

Fig. 45. An full overview of magnetization, step up and demagnetization with two different strategies using a chopper
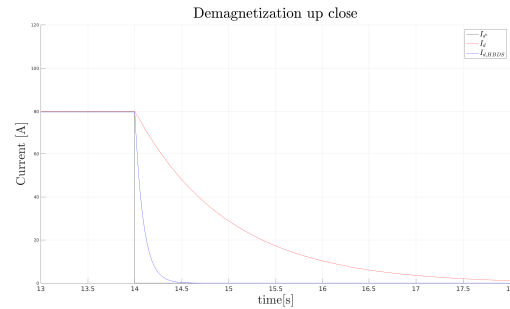

Fig. 46. A close-up on the two demagnetization-strategies. Clearly the HBDS results in a way more rapid demagnetization

The events shown in Fig. 45 are: At $t = 5s$ the VR is turned on, and the step is initiated at $t = 10s$. Up to $t = 12s$, hysteresis-control is used on the output-chopper. But at $t = 12s$ the control is changed to PWM-control where the duty-cycle is derived from $i_f - i_f^*$. At $t = 14s$ the demagnetization starts.

The large rise and ripple during the rapid step could obviously be an issue for the capacitors' rating. This problem could be mitigated by either using larger capacitors or ramping up the step over a given period of time. What happens now is that the PID-governing

$\hat{i}_s^*$ rises rapidly, dumping energy into the dc-link. Due to the highly inductive nature of the load, i_f changes slowly causing the extra current flow into the link. When i_f has increased substantially, also u_d falls to more acceptable levels. In an implementation a trade-off must be made between components and reaction-time.

About $t = 9,7s$ i_f reaches it's reference and the chopper becomes active, switching to keep i_f from rising. Since i_f now is considerable larger than earlier, this results in violent voltage-spikes and distorted current waveforms. This can be closer observed in Fig. 47.
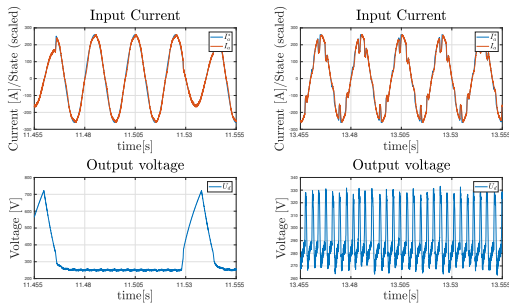
Fig. 47. On the left side is a snapshot taken when i_f is high and hysteresis-control on the chopper is active. On the right i_f is still high, but the control is switched to PWM-control.

By employing PWM-control instead, the switching-frequency rises dramatically and thus reduces the unacceptable ripples from the hysteresis-control shown on the left side. Theoretically the same effect could be possibly to reduce ΔI_f so much that one in effect would achieve the same switching-frequencies. But considering measurement equipment, the solution using PWM-control on the chopper should be considered in applications where the output-current rises to such magnitudes. The benedictory effect on voltage ripple can also be seen in Fig. 45 where this is greatly reduced. In both cases the current-waveform is somewhat distorted, although less in the case where PWM-controlled were applied. Some of the distortion should be possible to eliminate in the PID-controlled $\hat{i}_s^*$, tuning the PID with increased derivative gain. As is shown the notches are due to change in reference that the VR realizes, not due to breakdown in the functionality. The bad reference-generation is due to the sudden surge in u_d.

Two plots are shown of the demagnetization - of simply setting $S_{chop} = 0$ and letting the demagnetization current be dissipated in R_f. The much faster demagnetization shown with the blue plot is the result of applying a demagnetization resistor which the current is forced through (rather than the flyback-diode) when the demagnetization-signal is given. The demagnetization-signal to the VR is $\mathbf{S_{demag}} = 000$ to avoid any shorting of the phases during demagnetization.
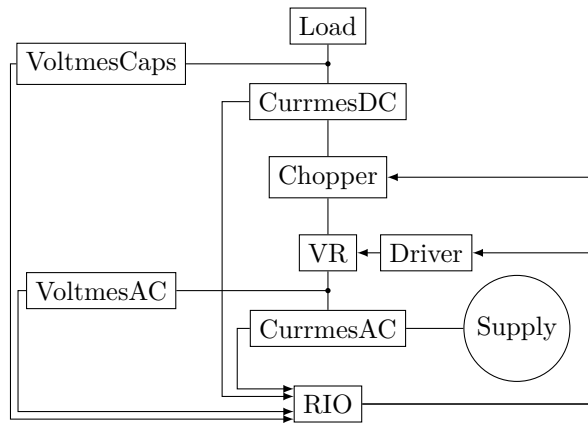

Fig. 48. Signals are shown as arrows. Although giving a large leeway regarding flexibility, the modular approach does lead to an large amount of connections that have to be done manually. Note that up to the VR there is a three-phase system shown as one single line.

VI. Demonstration

A. Introduction

The economical and practical limitations of the thesis forces a choice of parameters that isn't ideal for the comparison with a possible implementation at Svante testrig. Most notably was the current, and thus voltage limitations of the autotransformer feeding the rectifier. As shown in the flowchart 33, this results also in limitations on mains-voltages, and thus also the relative effect of voltage over semiconductors, e.g. diodes, will be more noticeable. These, together with other issues arising from practicalities will be thorough explained. Below a detailed description of each component and functionality will be given, but the overview can be seen in Fig. 48.
Due to several limitations regarding time and money as well as an unfortunate mishap that destroyed the driver-circuit, satisfactory results and further troubleshooting to rectify possible errors were not possible. During testing and implementation of the LabView-script, some occasional plots were stored. These will be presented and the deviation from the expected behavior will be explained. Several of the implemented solutions, e.g. regarding measurements, are not the best option available. A list of easy to implement improvements will be presented and should be heeded in e.g. a later master thesis on the same subject.

B. Components

1) Mains-supply: In lack of other easily available three-phase system, the grid supplies the mains. For this prototype to be tested properly and securely, two aspects needs to be addressed:

(a) Galvanic isolation to protect measurement gear and personnel
(b) A far lower voltage than grid voltage, $U_{grid} = 230V$.

The galvanic isolation is achieved through the use of three delta-star connected $1 : 1$ transformators. Three single-phase autotransformers were used to step down the voltages, two from Lubeck and one from Clairtronic.

U_{pri}	U_{sek}	$\hat{I}$
240 (nom)	$0 - 260$	3 A

TABLE XII: Autotrafo rating

To avoid inversion of one of the output phases, it was necessary to determine the polarity of the sockets. Since one of the autotransformers was of another brand than the other two, this was necessary to ensure that not one of the phases were inverted relatively to the other two. This would result in a phase-difference of $120° \pm 180° = \pm 60°$ between the phases and a non-symmetrical supply. Connecting every pair of autotransformators in parallel to a single phase and comparing terminal voltages with a multimeter solved this issue. Minimial terminal-terminal-voltage indicated the same polarity.

The schematic can be seen in Fig. 52. The supply-side of the transformer is shown in Fig. 51 and the three auto-transformers are shown in Fig. 49. A simple connection board were made by sockets and switches mounted on a plexiglas-board, shown in Fig. 50. This enabled quick switching of all or single phases on the supply. This proved a very practical functionality during testing and assembling of the test-rig.

Fig. 49. The three autotransformators. Note that the connection to the left on each autotrafo designates the ground on the secondary side, are all connected together. The motor in the background are not relevant for the demonstration.

Fig. 50. A basic, but practical connection board connecting the secondary side of the isolation-transformer with the autotransformers

Due to some differences in the internal connections of the two autotranformers from Lubeck compared to that of Clairtronic, it was also necessary to connect the negativ
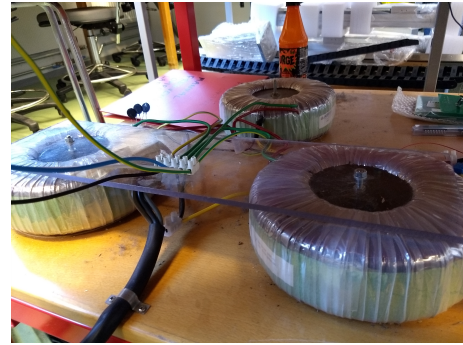

Fig. 51. Three ring-transformators are suppling the autotransformators with balanced, three-phase voltages.
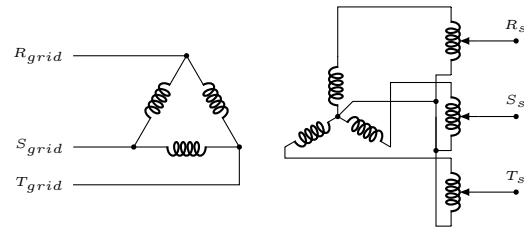

Fig. 52. A schematic showing the connection of the autotransformators

terminals on the secondary side of the three autotransformers to ensure symmetrical voltages. The autotransformators were outfitted with $2, 5A$-fuses, therefore no additional fuses were implemented in the other boards. In a improved design this should be a part of the VR-board.

2) The control-board: The control and information-gathering is done with a Compact Rio 9606 with Rio Mezzanine card NI 9683 from National Instruments. In the further discussion it is referred to as "the board". The board and controller has a wide array of functionalities aspects, only the ones relevant in building the control-application will be briefly summarized here. The board itself can be seen in Fig. 53

The architecture consist of an embedded real-time processor and a FPGA. The latter makes it possible to execute parallel task involving many IO-pins at a considerable speed compared to e.g. micro controllers [55]. They do however suffer from two constraints that were relevant for this applications:

1) Much faster data-acquisition than communication with host-computer
2) Limited amount of processing-power and storage

Issue (1) comes mainly into play during development of the application. Reading single readings into a scope from the FPGA resulted in way to few samples than necessary to determine voltage and current waveforms, as well as the response of the switching-logic to the input. Storing arrays of readings for displaying on a lower frequency than the board reads single values demands too much storage on the FPGA, taking (2) into account. The solution to this problems is to use a FIFO (First In, First Out)
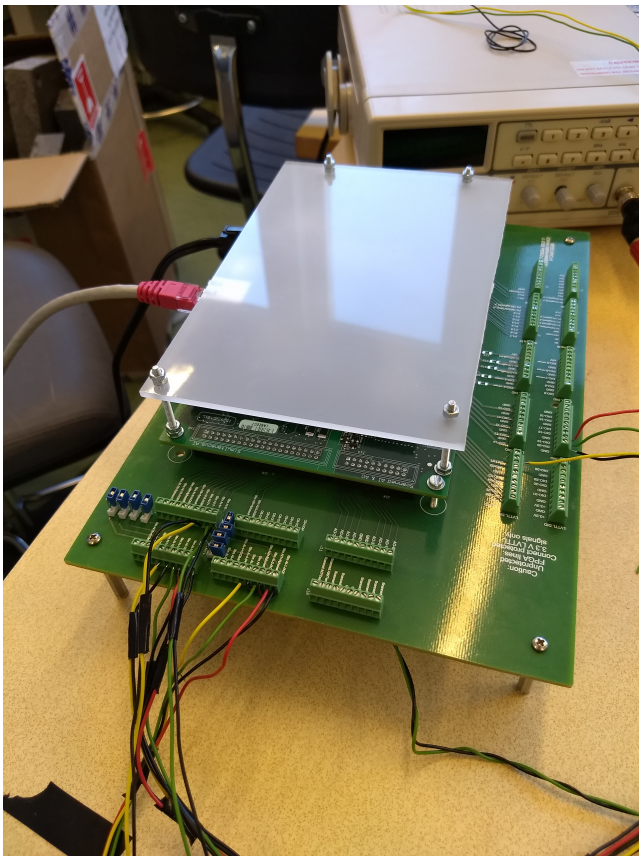
Fig. 53. The outputs on the right are the LVTTL-pins, the pins on the short side of the board are AI-pins. The cables are a UTP cable communication with the computer and a power supply giving $15V$ to the RIO.

buffer-memory that the FPGA reads into and a VI on the processor reads from.

The board has 16 simultanous analog input-pins (AI) with range $\pm 4,95V$ and also 31 Low Voltage $(3,3V)$ Transistor to Transistor Logic (LVTTL) pins. The range of the AI pins must be taken into consideration designing the voltage divider measuring the voltages in the rectifier. The LVTTL-pins are unprotected and faulty wiring may damage the FPGA permanently. This is a strong argument for using isolating gate-drivers in the circuit.
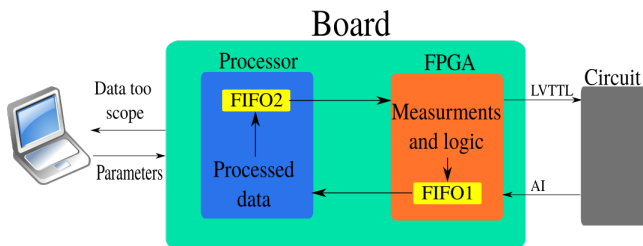
Fig. 54. A schematic representation of data flow in the system

Not all data types that are supported in the processor, are supported in the FPGA. Another issue is that each FIFO is data-type specific, implying that it can only transfer one designated data type. Since using several FIFOs in parallel in the same loop may cause some shift

in the read-signals sent to the processor, datatypes such as bool used to determine the state of outputs were cast to FXP (FiXed Point datatype) before passed to the same FIFO that the other measurements.

The simplicity of hysteresis-control does make the board an excessive over dimensioned component of the setup. Every block of the hysteresis-control can be realized with cheap and durable analogue electronics using mainly op-amps. A description of the circuitry can be found in standard textbooks such as [31]. Due to the scope of the thesis, these circuits however, were not designed.

For the same reason as with analogue circuitry a basic microcontroller could realize this control-strategy. This would however pose challenges should the control system be integrated with other systems using National Instruments equipment. The commercial available VR offered by Texas Instruments is controlled by a micro controller of considerable less complexity than the board.

3) Current- and voltage-measurements: Correct current-measurements on the AC-input are essential for a satisfying implementation of a simple hysteresis-current control. The DC-output current should also be measured to increased insight in the transient operation, but can in steady state be derived on the basis of output voltage knowing the field resistance as seen from eq. (9). The choice of current-sensor were motivated by a wish to keep cost at a minimum and using a measurement range as close to the demonstrations levels as possible. The current transducer used were a LM HXS 10-NP/SP3 which uses hall sensors and provides electrical isolation. Due to the $\hat{I}$

I_{nom}	G	$V_{out} - V_{ref}$
$10A$	$62,5\mu V/mA*$	$[0, \pm 2,5V]$

TABLE XIII: Key characteristics of the LM25 current transducer. *Gain were measured to $60,5\mu V/mA$ on two of four LMs.

ratings on the autotransformers the measurements would be taken far from the nominal ratings of the CT and thus the characteristics from the data sheet needed to be scrutinized. Some very small variation of G and a varying offset on $V_{out}-V_{ref}$ were found. These issues were accounted for through calibration and added offset in the VI. Using a standard oscilloscope noise with amplitude $5mV$ were discovered running a DC-current testing the CTs. The 12-bit $(\pm 5V)$ ADC in the RIO also sets a benchmark of how accurate the measurement is possible to achieve and will stack with this uncertainty as shown in Tab. XIV

Parameter	LM25	RIO ADC	Total
Voltage	$5,00mV$	$2,44mV$	$7,44mV$
Current	$83,0mA$	$40,5mA$	$123mA$
Perc. of I	$4,61\%$	$2,25\%$	$6,86\%$

TABLE XIV: Noise and consequence for current measurments using $G = 62,5\mu$ and $I = 1,8A$.
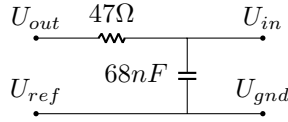
In addition there may come several unquantified effects

Fig. 55. RC-filter on the CT-output

such as instrument uncertainty. To improve readings two measures were investigated:

1) Averaging over several measurements in the LV-VI.
2) Using analogue filters on the CTs output

Experimentation with DC-current confirms the theory that averaging over a very large time period such as $0,1ms$ did almost eliminate all noise. But since the input is AC-currents and the switching logic is dependent on immediate current measurements there is a limitation on how long the averaging period may be. Therefore the solution involving filters were chosen instead. Some basic considerations is needed when choosing R_{filter}, C_{filter}:

The cut-of frequency and phase shift of the filtered signal in an of an RC-filter is given by;

$$f_c = \frac{1}{\omega_s RC} \tag{61}$$

$$\phi = -\tan^{-1}(\omega_s RC) \tag{62}$$

Presuming that the noise is distributed among a wide range of frequencies it is desirable to choose a cut-off frequency low, opting for a relatively large R_{filter} for a small C_{filter} (which is practical due to availability). But a phase shift would as noise result in a faulty current measurement and thus eq. (62) must be taken into consideration. Trial-and-error based on the eq. (61) and (62) resulted in the values shown in Fig. 55 with a considerable smoother signal observed in the oscilloscope.

Although, voltage measurements were less impacted by noise, also these measurements were filtered. Due to the low voltages of the demonstration set up, a simple voltage divider consisting of $R_1 = 10k\Omega$ and $R_2 = 1k\Omega$ were connected in parallel (star) to the mains. This results in a scaling factor of 11 when reading the values with the RIO. The RIO is more protected than using the neutral point of the isolation-transformers by using a virtual neutral point (denoted N_{virt}). If the voltages u_{abc} are not perfectly balanced however, this would lead to an neutral point voltage and somewhat skewed measurements. But since the measurements under visual inspections seem to follow sinusoidal, balanced waveforms this disturbances are considered minor. The same filter components were used on the output of the voltage divider to smooth the signal. Due to time issues and practicality, the components were placed on a small prototyping board rather than a custom PCB.

Although uncommon, a resistive voltage-divider may be used to determine U_{C1}, U_{C2}. In a real chip e.g. op-amp circuitry[4] could be utilized, but due to time constraints this option were not chosen. Extra care must be taken
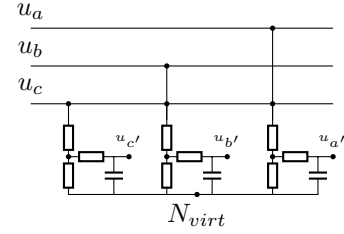

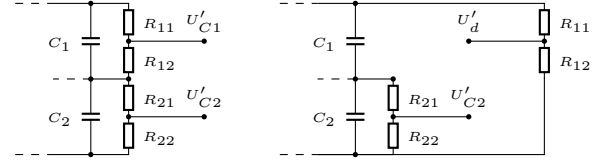Fig. 56. RC-filter on the voltage-measurements

Fig. 57. Correct way of connecting voltage divider to capacitor-link (left) and erroneous (right).

connecting the voltage dividers. Rather than putting one voltage divider over U_d and one over one of the capacitors and thus deriving the voltage on the other capacitor, two voltage-dividers of equal total resistance must be put in parallel with each of the capacitors. Not doing this would lead to an uneven loading of the capacitors and the voltage over the upper capacitor slowly increasing on the cost of falling voltage on the lower one. Even though the total output-voltage will be constant, this is not a acceptable situation for the VR.

Using the set-up to the left in Fig. 57 gives the correct voltages when measured with a multimeter. Connecting the outlets to the RIO however, the voltages get somewhat warped. The capacitors keep their original, balanced voltage, so this were not due to unequal loading or short internally in the RIO. It is suspected that the grounds of the AI-pins are only semi-isolated, and using different grounds will result in off-measurements. The solution to this challenge were to ensure equal loading of the capacitors, but only measuring u'_{C2} and using a second voltage divider measuring U'_d, as shown in Fig. 58

4) Gate driver: The IGBTs are not driven directly from the RIO, but from drive-circuitry. This is motivated by three items:

- The RIOs Low Voltage Transistor to Transistor (LVTTL) outputs can't supply enough current to switch the IGBTs.
- The drive circuit will function as a protective measure since the LVTTL-pins on the RIO are unprotected.
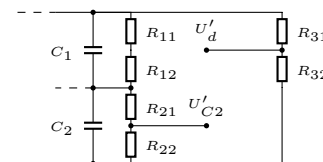
Fig. 58. Measuring U_d and U_{c2}. Note that U_{c2} is not directly measured, but will be derived from U_d and U_{C2}
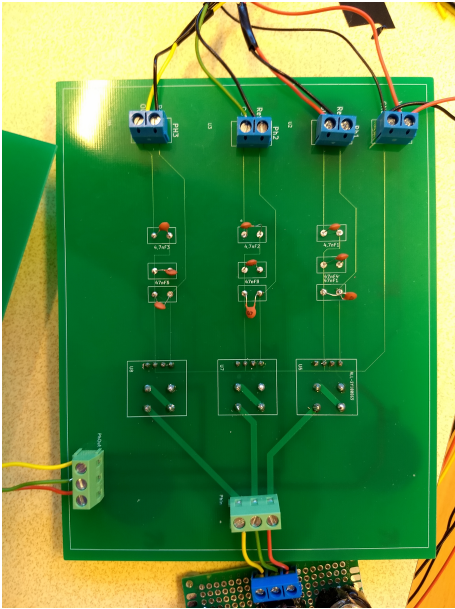
Fig. 59. Three-phase current-trancducer. The current-trancducers themself are on the underside of the PCB. This is due to an unfortunate mistake in the layout - the footprints of the current trancducers were placed mirrored. To save time and money the original pcb's were used but the current trancducers were placed on the underside so that the pins matched.
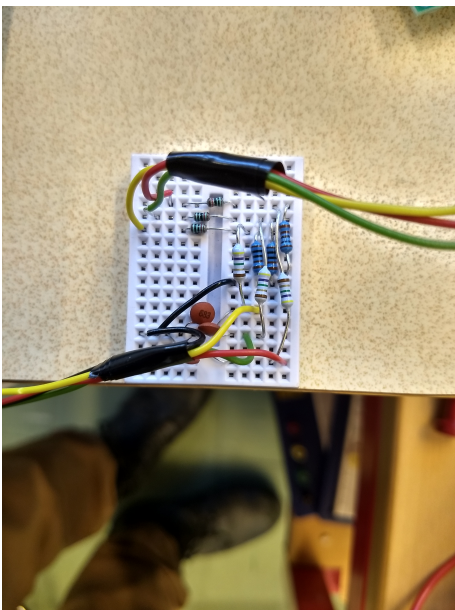

Fig. 60. The makeshift virtual neutral point, voltage divider and RC-filter giving the signal to the RIO from which u_s and thus reference for the current is derived.
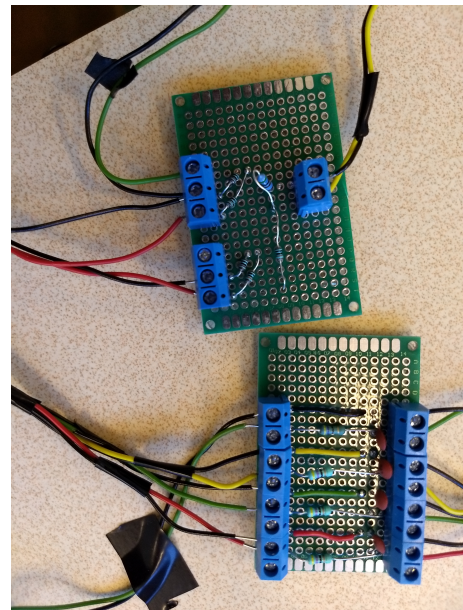
Fig. 61. The upper board contains the voltage dividers for returning u_d and u_{c2}. The yellow wire returns u_d, while the red and black wires are connected to relevant points in the dc-link and the RIOs AI-pin.

- The emitter-pins of the IGBTs are floating.

The last point is essential - to turn on the U_G needs to be $U_{GE} > \approx 15V$ to complete turn-on of the IGBT. But observing Fig. 16, the emitter-voltage will be at $\frac{U_d}{2}$ when the $i_x > 0$ and $S_x = 1$, given that the drive-circuitries ground is connected to the negative terminal if the VR. This problem also arises in e.g. a H-bridge where the high side transistor experiences a high emitter-voltage and thus needs external circuitry to turn on. Inspired by such an application a full-bridge driver IC utilizing bootstrap-method, using only the high-side output were first considered. But observing the workings of the bootstrap-circuit, a successful operation are doubtful. When the switch is off, the emitter is not tied to ground, unless the drive circuits ground is directly wired to the emitter-pin which in turn would inhibit the operation in "on" state. Thus the bootstrap capacitor will never be charged. For illustration-purposes a schematic of the original planed bootstrap-driver is shown in Fig. 76

Important to note is that in contrast with a traditional half bridge drive configuration [27], the drives may not use the same power supply directly. This is due to the fact that the driver cannot have a single ground for all three switches. This would entail connecting the emitter-pins together and would on some instances would lead to an shorting of two phases. This is shown in Fig. 63 with distorted input-currents and dangerously high current between phases. The isolation between signal side and power side is achieved using optocouplers (HCPL-3120-000E). A brute way of ensuring three separate voltage sources is to use three times two 9 V batteries supplying the necessary 15-30 volts to the optocoupler. A more traditional way is to use a single power supply and separating this into

three separate, floating supplies using a DC-DC converter (IML02 from XP power). A drawback in this solution is the upper limitation in supply current. Whilst the optocoupler can supply 2.5 connected to a battery, the DC-DC converters is 167 mA, effectively increasing the turn-on time of the IGBTs. Higher rated DC-DC converter is commercially available, but not in the price-range of this demonstration. Therefore a board enabling both the use of batteries as well as dc-dc converters were designed and is shown in Fig. 77. A picture of the assembled driver-chip using the dc-dc converter rather than batteries can be seen in Fig. 62.
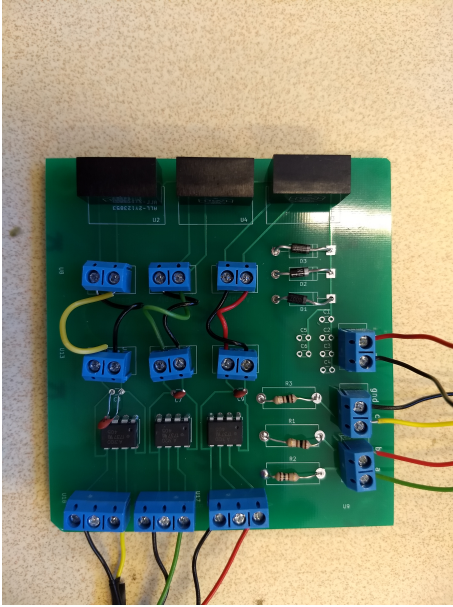
Fig. 62. The driver-board. The black boxes in the upper part are the dc-dc-converters. The diodes and resistors stems from the application notes in the dc-dc-converters and optocouplers.
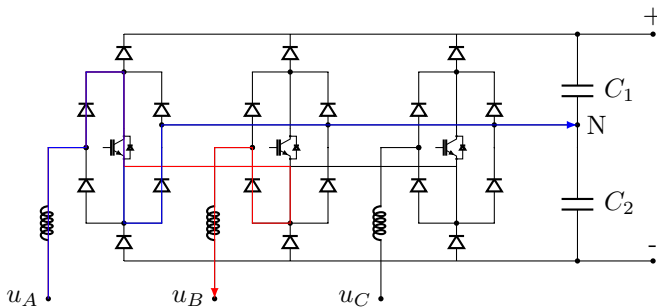
Fig. 63. Sector 1, $\mathbf{S} = [100]$ and $sign(i_{abc}) = [+ - -]$. The blue path shows the correct current path, the red one the faulty path if the emitter-pins were to have a common ground. From u_A to the emitter-pin of Q_A the paths overlap.

5) PCB-boards: The boards were designed using KiCad opensource software. Rather on compactness, the focus were put on redundancy regarding both track width and ease-of-assembly. Due to the suspected marginal effect this will have on the signals using such large separation of the

tracks, cross coupling and EMI-noise were ignored in the design. Considering the lack of experience of the author, a modular approach were chosen rather than putting all functionality on a single board. This enabled modification of a single components or boards in the case of errors. This proved useful on several occasions, e.g. after wrongful soldering on the current transducers. On the downside, such an approach produces the need for considerable wiring between the components.
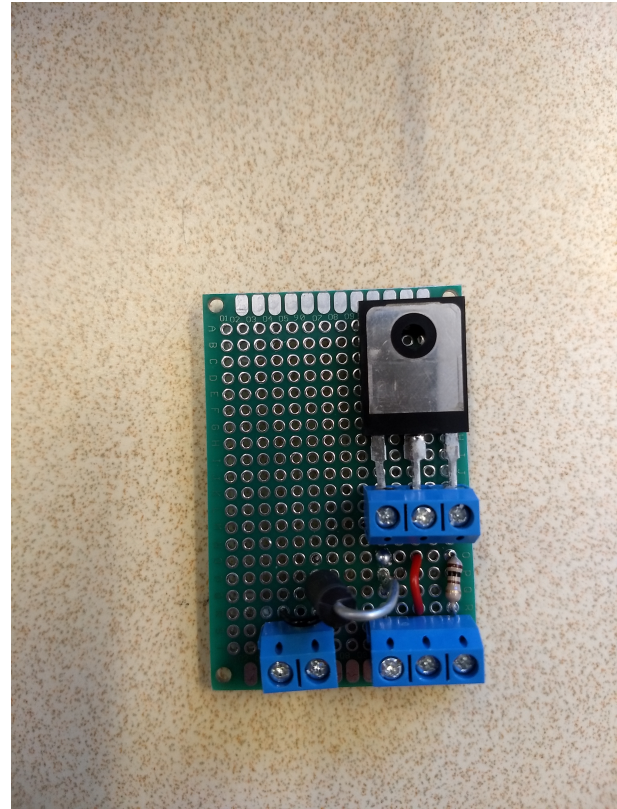

Fig. 64. The chopper used on the output. The resistor is a gate-resistor for the IGBT which in the same manner as the VR can be readily switched. The diode is a freewheeling diode ensuring that current may continue to flow in the inductive load during "off"-portion of the choppers duty-cycle.

6) Load: The RL-load consisted of an inductance and a variable power-resistance. In the part of the demonstration where no-chopper were used the R were set high (20Ω) to limit the discharge of the capacitors. The load can be seen in picture 66

The inductance were scraps from a soft starter that have been taken apart and consists of three separate windings which shares iron core. The inductance of each coil were estimated connecting a known capacitor-value in parallel with one of the coils. A voltage signal with known and variable frequency were added and the voltage over the components were observed in a oscilloscope. A schematic over the connection is seen in Fig. 67

Noting at which frequency the peak were the highest, the formula for resonant frequency 63 were used to estimate L.

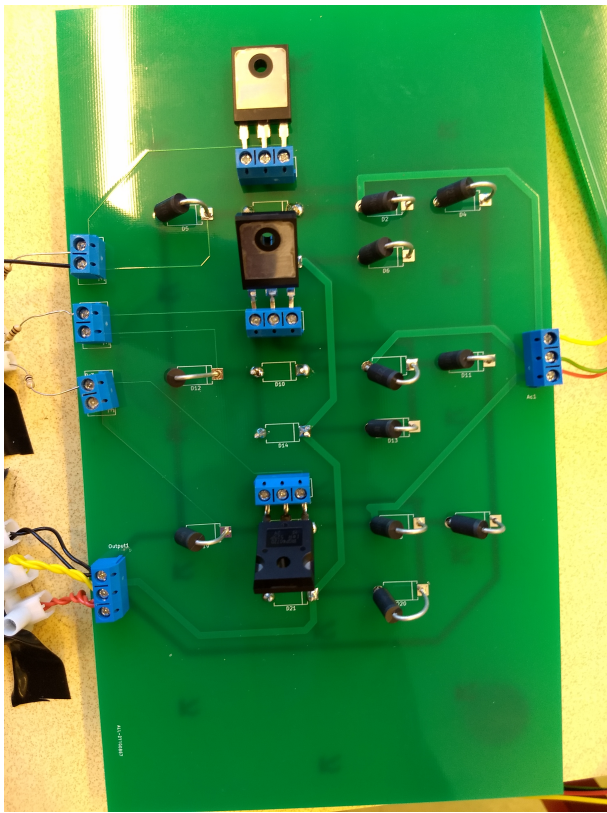$$f_{res} = \frac{1}{2\pi\sqrt{(LC)}} \tag{63}$$

Fig. 65. The actual implementation of the VR. On this picture there seem to lack six diodes - they are mounted on the underside. The reason is to have space to switch out the IGBT. After an unfortunate mishap were use of gate-resistors were not in place, three IGBTs burned out and a whole board had to be discarded. By rather using screw-terminals, they can be easily exchanged should a similiar mistake be made again. To have have room some diodes had to be put on the underside of the VR.
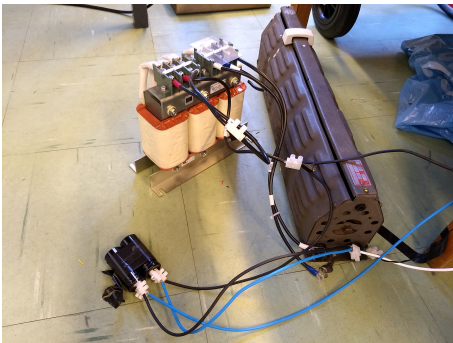

Fig. 66. The RL-load used

The estimated inductance per coil were $L_{coil} = 160mH$.

C. Labview implementation

The programs in Labview are drawn as flowchart. These programs are called Virtual Instrument, (VI) and can be compiled into the FPGA or written directly to the processor on the board. Best practice is to read data from the FPGA through a VI on the processor which get passed data from the VI on the FPGA through a FIFO. The VI on the FPGA will be refered too as FPGA-VI and
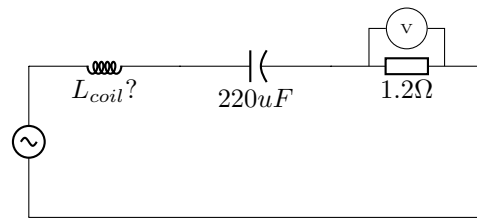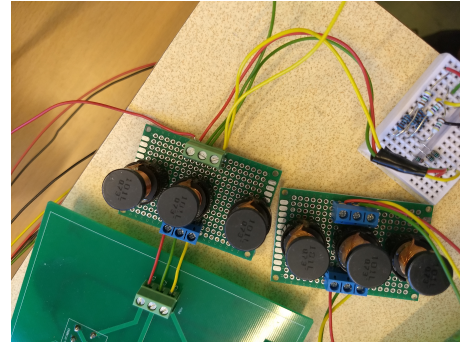

Fig. 67. The circuit used to estimate L_{coil}

Fig. 68. The inductances on the input, each $1mH$. Six individual inductances were bought test with differente values of L_s. In the results recorded, only $1mH$ were used. To the left in the picture is the three-phase filter inductance connected, to the right is the second mini-board for illustration.

the one on the processor as RT-VI. Screenshots of the flowcharts can be found in the appendix for readabilities sake.

The naive, proof-of-concept VIs that were implemented left much memory on the FPGA and a fair amount of processing power also, as shown in Tab. XV

Resource	Percent used
Tot. Slices	54,1 %
Slice Registers	17,6 %
Slice LUTs	38,1 %
Block RAMs	4,3 %
DSP48s	81,0 %

TABLE XV: Result of the most complex VI that were implemented on the board.

It is expected that these numbers also can be improved optimizing the VI for speed and space. This indicates that the RIO will have plenty of capacity to control other processes simultaneously while controlling the VR.

1) Override and safety measures: To help in troubleshooting and analyze of the behavior, the functionalities of the control-loops were implemented with a great deal of controllability. This was realized through following:

- The signals governing the chopper were given too two different LVTTL-pins - one where hysteresis-control were applied and one where PWM-controlled were used. In this way one could easily switch between the two control-methods. At a later this should be done in the control board rather then switching pins.

- The switching-logic of the VR may be over overruled.
  - In hysteresis-control, this entails passing a $\mathbf{S} = [000]$ signal to the switches, in effect making the VR a diode bridge.
  - In PWM, due to the nature of the realization, a duty cycle array containing $\mathbf{D} = [0\ 0\ 0]$ were passed to individual realization of the duty cycles for each phase. As above, the result is a diode bridge.
- Care were taken that it were the signals from the switching logic rather than the ones resulting from the override were passed to the RT VI. In this manner, it was possible to start up with the VR in default diode bridge mode and scrutinize what the immediate response of the switching logic would be. This functionality were used to detect if any of the parameters governing the switching logic were wrongfully entered.

The main goal of the above precautions were to avoid an error resulting in the null-vector $\mathbf{S_0} = [111]$ over time. This would cause a shorting of the three phases and blowing of the fuses. Designing an automatic catch-system seems complex since $\mathbf{S_0}$ is a part of the switching-logic and not banned altogether from the operation. In a proper implementations it should in any case be the current-levels themself that triggers a reactions, not the amount of time $\mathbf{S_0}$ has been on.

2) Reading and displaying data: The principle of reading real-time data from the circuit works as follows: In the RT-VI an array of a given length of values is queried from the FIFO. This length is given as e.g. "PhElement" in Fig. 89. This is multiplied with the number of variabels that is passed through this single FIFO such that PhElements are queried *for each variable* that is passed. Due to the nature of the FIFO, some array-operations are needed to convert the data flow into separate arrays for each variable. These arrays are then passed to a graph displaying them in one plot for comparison. An drawback with the current system is that even though the data is displayed correctly relative to each other, they contain no timestamp.

3) Control-loops: Three different control-loops were briefly testet: Hysteresis and two implementations of PWM-control. The hysteresis-control can be seen in Fig. 91. This utilizes the build in hysteresis-block from NI and modifies the result for current polarity using a XNOR-block. The output of the NI hysteresis block is converted to boolean with a simple comparison block, but might as well be used a cast-block from the NI-library. This is typically one of many small measures that should be taken in further work to improve the VI.

The IR was implemented in Fig. 90. The sign of each input current and -voltage is compared and the reference is multiplied with the result (0 or 1) of boolean operations to zero out the reference should the polarities be different.

The first PWM control loops, suspected to be a bit slow is seen in Fig. 94. Rather then in time, the period is defined in numbers of cycles. During operation the average time of such a cycle is considered to be constant, and thus may be used as basis for the period of the PWM signal. However, to improve on this a timed loop using the onboard clock should be used. Some technical problems regarding the calculations be compatible with the limitations of such an timed loop needs to be overcome, but this is far from an insurmountable task. The workings is as follows: A given number of iterations (period) is given. As long as the current number of iterations are lower then the period times the duty cycle the output is turned on. The remaining iterations the output is turned off. When a period is passed, the counter of iterations is reset to zero. In both methods the PWMs duty-cycles were derived from the form of the input-voltage. The absolute-value of the input voltage scaled to correspond to the given amplitude ($\in [0, 1]$) were taken as input.

The second PWM control-loop is the same as used for the chopper and can be seen in Fig. 96. Here, each phase has it's own, individual loop. The output is turned high for the period times duty-cycle and low for the rest of the period. This is realized with a stacked sequence and wait-commands. The use of stacked sequences/wait-function warrants that this operations has to be conducted in an individual loop so to not halt the other operations due to waiting.

It is important to note that this PWM-implementation is missing a key element for ensuring $pf = 1$ on the VR. A phase shift of the reference voltage compensating for the input-inductance is necessary. Due to the scope of the thesis and complexity of implementing such a shift, this were not done here. A closer description of this problem is described in [16].

4) Elements missing for a fully working VR: In this dummy-implementation the amplitude of the input-current were set manually - as well as many other parameters. In a finished prototype the following is a minimum for what needs to be in place:

- A feedback control, e.g. PID governing the input-currents amplitude. The input may be the dc-link voltage or the actual output-current in the case no chopper is used.
- Derivation of parameters from component values rather then testing manually.
- Hardcoded gain from sensors.

5) Easy to implement improvements: In building a own, designated VR some small, but valuable improvements should be done firstly:

- Fix PWM to using timed loops for control of period. This should also be placed in a sub-VI in the same manner as with hysteresis-controls.
- Rather then using the voltage from the mains as reference, the build in sine-signal-generator should be used. A PLL or other syncing methods must be used to sync this signal with the supply voltage. The benefit of this solution is:
  - No use of scaling the input-signal for changing amplitude - the reference will then have a set

amplitude of e.g. 1 that will be scaled according to intended amplitudes (either duty-cycle or reference currents.)
  – Smoother signal
  – Independent on possible disturbances in the measurements due to switching. This was not an issue in this setup since the supply was stiff, and measurable, but this may not be the case in a the implementation in a machine.
- Use sliders for control rather then numbering input. This makes it easier to identify limits of each parameters and to avoid mistakes.
- Implement a shut-down functionality in case of too large currents being drawn to avoid being dependent on the use of fuses
- A time stamp should be used in the reading of values.
- In case of still noisy current measurements, averaging of values in the RT and passing them back to the PFGA is an option that should be considered.
- Moving the control-board from the FPGA to the RT and passing the parameters through a FIFO. Slower means of passing data between the VIs may be easier to implement.

D. Experimental setup

The following values for the external components were used. The capacitors were chosen much larger than necessary to mitigate any possible issues with to large voltage ripple on the output. The input-inductance were chosen on grounds of initial simulations giving satisfactory results of the circuit in Matlab Simulink.

C_{link}	$1000uF$
L_s	$1mH$

TABLE XVI: The parameters for the external components.

1) Event: The dc-dc-supplies were mismatched to the optocoupler and the IGBT, having an maximum current output of $167mA$ and maximum power of $2W$, in contrast with the optocouplers upper rating of $2,5A$. During testing with PWM-control, the dc-dc supply became notable warm. This was suspected to be a consequence of a high switching frequency and thus a larger toll on the dc-dc converters to turn on/off the IGBTs. Due to financial reasons and the fact that the demonstration circuitry only were meant as a proof-of-concept, this design flaw weren't mitigated. At one instant the PWM-governed drivers were allowed to run for several minutes, causing large heating of the dc-dc supply. After this incident they were broken and could not deliver the necessary 15 volts to drive the IGBTs. Having some preliminary test-data little time left until deadline, it was decided to cease the practical implementation and rather prioritize using time testing a purchased industrial VR at a later time after the thesis. As a results of this the focus on this sections is one the qualitative qualities such as waveform rather than more detailed analysis regarding e.g. modulation factor and such.

2) Results: In the plots below a black line indicates a running mean of the signal. The bin-size were 20 and the total signal were 1200 data points.

From Fig. 69 several conclusions can be drawn. The green plot, showing the S_a shows related to the reference and actual current that the switching-logic works. However, the very large ripple (red plot) indicates that one out of two measures should be taken:
- Increase input inductance.
- Reduce ΔI_s to speed up switching.

The notched form of the reference is due to the adding of the ΔU_c-element rather than rugged reading of the input-voltages. As shown in the lower plot this causes $\Delta U_c \approx 0$ and the workings of the proportional control be considered a success. The major issue and shortcoming of this result is the very large overshoot that occurs after each zero crossing. Even thought the switching reacts correctly and turns of during the overshot, the current rises to way to large levels before being reduced. Due to the event this was not scrutinized closer at the moment and recordings of e.g. the currents in the other two phases at the same instant weren't obtained. Possible remedies are listed in tab. XVII.

Cause	How to check	Suggested remedy
Too small L_s	Test with larger L_s	Increase L_s
IGBT aren't turned on	Record U_{CE}	Increase current output of driver
Interaction with other phases	Record all phases simultaneously	Check for bug/error in VI. (Should be equal)
Control too slow	Compare with ocilloscope	Reduce ΔI_s Speed up VI

TABLE XVII: Possible ways forward to remedy current overshot. Another very interesting parameter to measure would be i_M. Given the modular nature of the prototype this should pose no big challenge.
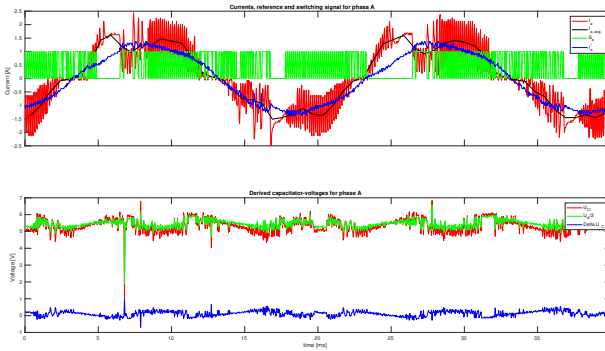
Fig. 69. Using hysteresis-control

Knowing the issues regarding measurements of input currents, a simplified and not quite complete PWM control of the VR were briefly applied. This control-strategy isn't directy dependent on measuring the currents. The phase shift over L_s were ignored and u_s, as in the hysteresis-control were used to shape a reference. The first implementation may be seen in Fig. 70. *On average* a sinusoidal current signal is achieved, but this is clearly non-continuous mode. Another issue is that the implementation of the IR gave erroneous results. When the current is negative, it will due to noise and non-continuous mode momentarily be (barely) positive. Since the reference is negative at this moment this will cause the IR-regulation to act and cause unnecessary and unwanted ripples in the duty cycle. In the PWM-VI, the regulation of ΔU_C were disabled on the basis of that it aren't needed in an ideal system [16] and there were timing-issues in the FPGA. This could also be resolved by splitting up the while-loop in question in several loops or making the calculations more effective, but initially this control were deleted and planned implemented if needed. From Fig. 70 it is clear that this weren't necessary since ΔU_c are kept quite small.
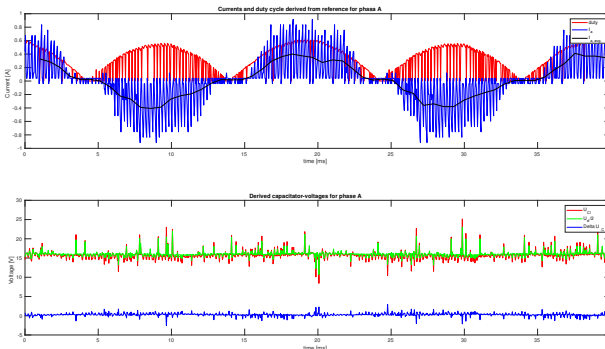
Suspecting that the former implementation of PWM limited the switching speed and thus increasing ripple, a new implementation were chosen. The result can be seen in Fig. 71. The control manages to keep the system in CCM. The large current-ripple and not quite sinusoidal waveform are still issues that must be addressed. The former should be quite straight forward, the distorted form must be scrutinized further. It seems that there is a bump right before the zero crossing that originates the distortion. Without further measurement it is challenging to determine what causes this.

Suggested improvements of the PWM-control are:

- Control number type of the duty-cycle variable to get more continuous control-signal. It is obvious from Fig. 71 that the duty-cycle signal is discretized with an unnecessary low resolution.
- Improve IR-control so it doesn't fire wrongfully due to noise from the current-measurements.
- Using best-practice PWM-loop for each phase individually rather than a makeshift loop for all three in one loop.
- Increase L_s or f_Δ to reduce current ripple.
- Implement phase-correction though using build in sine-generation on the FPGA and synchronizing this to the main voltage before shifting.

By adjusting the duty cycle or the reference current on the output it was possible to adjust the output current. This didn't change the behavior of the VR shown in the plots above. This is as expected since the DC-link were of considerable size and the chopper is placed after this link. The AC-side thus saw the same semi-constant DC-link voltage regardless of the immediate state of the chopper.

3) Suggestions for improved prototype: Although many of the suboptimal solutions of the demonstration set-up were chosen out of financial and time-limitations, there are several measures that in hindsight that would improve the without any more additional costs or design-challenges.

Instrumentation

- Using op-amps/buffer circuitry rather than resistive voltage divider for measuring the voltages both on

Fig. 70. A lower PWM-switching-frequency causes non-continues mode but sinus-resembling waveforms.
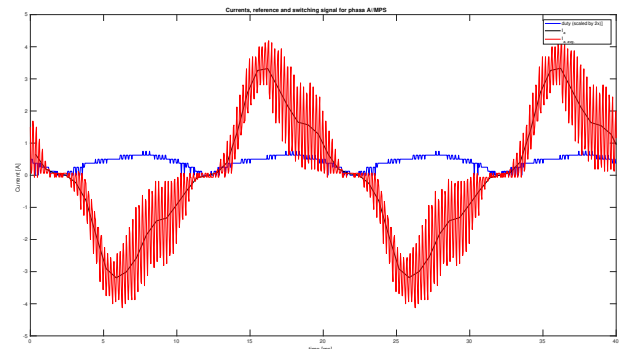

Fig. 71. Implementing PWM with a higher switching-frequency

the input and over the capacitors.

- Investing in less noisy hall sensors for the current measurements, possibly look into other methods. In the final design, hall sensors are the probable choice, but for a test conducting only a few amps there may be less noisy alternatives.
- Implementing a better filter than the basic RC-filter used in this prototype.
- Also measure i_M. This is not needed for control directly, but is still a key value for troubleshooting in control-design.

PCB-design

- Although the modular were practical in this first attempt, it resulted in an unnecessary amount of wires. Sensors for current, voltage, drivers and so forth should be contained in one PCB, despite the possibility that the whole board possibly must be adjusted and then re-ordered.
- The necessary terminals should enable exchange of DC-link and filter-inductances. Specially the latter is a key value that may be varied in the rig in mind, and should therefore be interchangeable.
- The size of the PCB could be dramatical decreased by reducing the spacing of the components that in this implementation were much larger than necessary.

Components

- In [44] a magnetic, rather than optical coupling for the drivers are recommended. Although not absolutely necessary, this should be considered.
- Matters must be taken so that the driver can stand high switching-frequencies, alternatively limit this in the VI. In any case the design of the driver should be conducted more carefully so to avoid events as with this prototype. Possibly designated IGBT-drivers ICs should be used rather than using the makeshift solution with isolated dc/dc supplies and optocoupler that were under-rated for the task.
- Although over-rated solely for this task, the RIO-board is a good tool that also could be used to run other processes in conjecture with the VR at the same time. In later efforts, a working Xilinx-compiler should be in place rather than using NIs cloud-compiler. Its long compilation time makes development of the FPGA-VI arduous.
- The load should consist of a variable inductance as well as resistance. The set-up in this demonstration didn't allow for continuous adjustment of L_f which limit testing of the operation of the VI.
- The components (L_s, L_f, R_f) should be properly scaled according to the data at the Svante testrig. This was not the case in this set-up.
- L_s should be a variable inductance so the effect of varying this parameter may be observed.
- Although not crucial, a three-phase autotrafo with higher current rating would eliminate the need for manually balancing the three phases at each adjustment of input-voltages, as well as increasing the

possible range of testing.

VII. Discussion

A. Suitability

One of the hallmarks of the VR is that of it's high power-density [44]. One of the reasons is that it's demand for relatively small filter-inductances [14]. The main idea, regardless of rectifier, is to utilize the main winding inductance rather than applying these externally. Since simulations shows issues with *to large L_s*, there may be other active rectifiers that are more suited. However, compared to the thyristor bridge, it has obvious advantages. The main drawbacks are:

1) Unidirectional powerflow
2) Chopper on output is needed for full field-forcing capability
3) Need for drive-circuitry
4) More complex control

Item (3) and (4) are minor and should pose no greater challenge for an experienced designer. Item (2) could be a useful implementation regardless of the VR or other design is chosen. If the HBDS-solution is utilized for demagnetization, the chopper could also work as a breaker, keeping more energy from the mains to be delivered to the field winding in the case of demagnetization. This could also be achieved by three-phase ac-breakers from the mains windings. In the case of EMs on the stator, a DC-breaker on the stator could also be an alternative.

The unidirectional powerflow is only an issue if the HBDS-solution isn't deployed, since demagnetization is the only instance where the bidirectional powerflow would be necessary. The work regarding this patent that is presented earlier in the thesis have shown such promise so that it is reasonable to assume that it will become one of the standards in future RPE-systems. In this case, the need for bidirectional powerflow regarding demagnetization will no longer exists.

As already discussed in the simulation-part of the thesis, the size of the input inductance could be a challenge. Without the possibility to switch between series/parallel-connections in Svante the VR would not look like a promising alternative. However, with wound exciter rather than using PMs, this problem seem to be less of a concern. As long as these conditions are taken into considerations the VR should be well suited for excitation-application in RPE. Retrofitting the VR to existing excitation-systems may pose problems if the feeder is of a nature that doesn't let the VR operate optimal. It should be noted that given a to large L_s, the VR doesn't completely fail to operate, but it's operation falls below what is expected regarding current form on the input.

Although not analyzed in this thesis, the VR has a efficiency of 98%[14]. Considering the small amount of total energy that the rectifier handles this should be considered more than adequate.

B. Other control-systems

Even thought hysteresis-control were analyzed in this thesis, PWM might as well be the preferred control-strategy for the VR. The main advantages over hysteresis-control are:

- Determined switching frequencies makes dimensioning of the component and ripple easier and more predictable.
- High-quality current sensing not as crucial
- Predictable EMI and harmonic content, thus making filter-design easier.

Hysteresis-control is however easier to implement. But since the system in all probability will be controlled by a board of qualities like the RIO, this should pose no significant problem. In [16] a few of the more complex control strategies, such as model predictive control, are briefly reviewed. Even thought these have been applied with great success, they entail greater complexity and thus possibility to fail. Seeing that the VR performs satisfactory in simulations with the most basic of controls only, this should be attempted implemented before possibly more complex methods than PWM and hysteresis is applied.

C. Economic considerations

The excitation system is handling very small amount of power relatively to the synchronous generator as a whole. The same considerations goes for the costs; the rectifier of the excitation system is a very small portion of the total investment costs tied to a synchronous generator. Nonetheless, using a VR over a thyristor bridge will entail some extra material costs. A comparison of the necessary components in three comparable solutions for RPE is shown in Tab. XVIII. Minimum requirements are control of output-current/voltage and the ability to demagnetize with a lower time constant then that of the field winding.

Rectifier	Components	Driver	Design
D. bridge	6 diodes Chopper HBDS	No	V. simple
Th. bridge	Thyristors	Yes	Simple
VR	18 diodes, 3 IGBT/Mosfet, 2 Caps, (Chopper) HBDS	Yes	Complex

TABLE XVIII: Comparison of the number of components. Not absolutely necessary components are shown in parenthesis.

It is clear that in simple hardware-expenditure, the VR is definitely the most costly of these three alternatives. Since no commercial product for this rating and application is available, considerable design-costs need to be accounted for. If the VR as topology were to be used in the industry, these cost will naturally fall considerable. Up to this point it is hard to justify use of the VR on pure economical grounds. Not considering design-costs however, two competing hardware investments will need to be considered: Does the larger costs of the VR be justified by the need for smaller mains inductance?

The lifetime of capacitors and semiconductors are dependent on the load the components will be experiencing and external factors such as cooling and mechanical stress. An analyze of these factors are outside the scope of this thesis, but considering typical components that may be used the VR will entail more maintenance on the rectifier. This is due to its use of capacitors, by far the most short-lived out of diode, IGBT [12] and capacitors. Considering e.g. a $100uf, 250V, 25A$ polypropylene capacitor from EPCOS, the capacitor would have a rated lifetime of about 10 years. In any case, the exchange of capacitors on such a timescale doesn't pose a significant economic cost and could be done as a part of a general maintenance of the machine and RPE-box.

D. Alternatives to the VR

Apart from the traditional solutions using diode- or thyristor bridge in the rectification, other PFC rectifiers may be considered. In [14], a comparison between the four most promising topologies regarding (relative) simple control-strategies, power density and component-requirements.

A Six-Switch Boost-Type PFC Rectifier
B VR
C Six-Switch Buck-Type PFC Rectifier
D Swiss-rectifier

For readabilities sake, the relevant findings for the application is discussed here. Of the four topologies, A and C are uni-directional, although the latter only if the output voltage may be inverted. As the problem for this thesis states, one of the motivations for scrutinizing the VR is the possibility for not adding filter inductances and solely depending on the inductance of the mains windings. The same advantage goes for (A), but not for (C) or (D). There an additional filter-inductance has to be placed on the output. The bi-directional power-flow is an important benefit of alternative (A) and (C) over the VR since this enables rapid demagnetization by inverting the voltages. The complexety of the control of the topologies are comparable. Also being boost-type, alternative (A) seems the most promising alternative topology to inspect further for this application. It were found to have a bit higher losses than the VR, but considering the great advantage of reverse power-flow this seems like a good alternative. In other aspects the VR and alternative (A) performed similarly.

Another, quite recent proposal is the one-switch VR. In [49] the topology, workings, simulation and experimental results are shown. Utilizing the neutral of the mains, two diode bridges, the split dc-link of the VR, two additional diodes and a *single switch*, the one-switch VR manages to

satisfactory results regarding power factor correction and sinusoidal input-currents. Although not yet as thoroughly tested and analyzed as the VR, this seems due to its very sparse use of active components as the most promising topology for the RPE-application.

E. VR versus thyristor bridge

The main advantage of the VR is the capability of current shaping on the input, and thus also power-factor control. As mentioned earlier in this thesis, this is an advantage regarding rating of the supply main windings. Other beneficial effects may also arise from using a low-THD, high pf solution such as the VR. Although the thyristor bridge has a greater control of u_d this comes at the expense of distorted input currents - and voltages. For illustration-purposes the set of parameters corresponding to the re-connection of the mains windings were simulated using a thyristor bridge with firing angle $\alpha = 30°$. The model can be seen in Fig. 87. Output voltages and current are shown in Fig. 72. A detailed analysis of thyristor bridge for excitation-analysis can be found in [30]. The input-stage is of greater interest for a comparison between the VR and thyristor bridge. Voltage and current forms on the input are shown in Fig. 73. The distorted current form is the cause for a high THD and low pf.
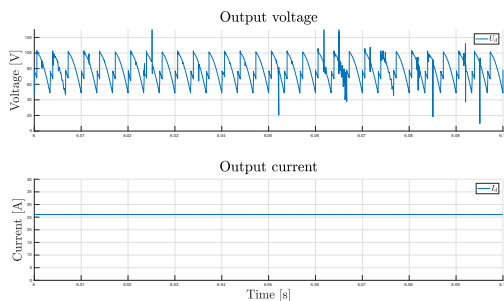
Fig. 72. The output of the thyristor. The current is constant in spite of the large voltage ripple due to the large windings inductance.
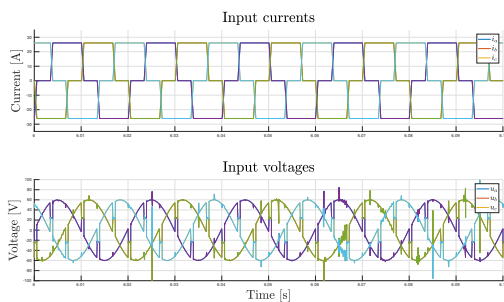
Fig. 73. The input characteristics. Note that the current are of a somewhat different form than typically shown for a thyristor bridge. This is due to the inductive nature of the load that forces semi-constant output-currents. In the plot of voltages the notches can clearly be seen. They occur at each commutation, four times each period per phase.

pf	$THD_{ph,V}$	$THD_{ph,I}$
0, 85	0.25	0.3

TABLE XIX: Measures of power quality of the thyristor bridge

The voltage-notches of the thyristor bridge which is dependent on L_s and α may cause torque pulsation [15], increased heating in the windings as well as disturbing other utilities such as measurement equipment [28]. Although the latter would also be an effect in the VR due to high voltage THD, the torque pulsation seems unlikely to be an effect of the distorted input-voltage of the VR. This is due to the non-periodical character of the distortion causing this THD. This is caused by the switching that will occur up to several hundred times per cycle (depending on the hysteresis band) and be more like to noise. This stands in contrast to the voltage notches that occurs with at regular intervals as seen in Fig. 73. A clear advantage of the thyristor bridge is it's simple design and ability to reverse field voltage in a sixth of a electrical period. From the results in this thesis, a conclusion regarding which topology is not possible to reach. However, the VR has a greater controllability that may also be utilized by other application, possible e.g. mechanical stabilization though briefly adjusting the input currents. But more research is needed in this field to conclude, and until the VR is tested and implemented as RPE it is hard to determine the superior topology of VR and thyristor bridge.

F. Additional circuitry

Additional circuitry adds to the already large complexity of the VR, compared to e.g. the thyristor bridge. But as shown in the simulation-part of the thesis, this doesn't necessarily entail more complex control. On the contrary, a chopper on the output will leave the VR only to ensure a sufficient (but with a large tolerance) voltage of the dc-link and sinusoidal input-currents. Since it is the chopper which governs the output-current and average voltage, the VR is free from a constraint. The simulations also suggests that the chopper is not only beneficial, but an absolute necessity to fulfill the standards regarding ceiling voltage. The chopper could also act as a DC-breaker, making AC-breakers on the input superfluous. The capability to rapid switch off the power to the field windings is important to make the operation safe in case of faults.

Allowing only uni-directional power flow the VR on its own is left with no other means of demagnetization than to break of the supply voltage either through AC breakers on the input or DC on the stator side inducing voltage into the mains. The demagnetization will have the time constant of the field winding. As shown in Fig. 46, not using HBDS results in a demagnetization time of several seconds. Although not specified in FIKS, it is reasonable to consider this a far to slow. In the case of short on the stator-side which isn't caught by other protective equipment, the stator windings will be fed

power for several seconds before the field windings is completely demagnetized. So if not absolutely necessary, the demagnetization circuitry would increase the safety of the operation and possibly also contribute to avoid damage in case of faults.

Since communication-link and housing already is in place to house the VR, the cost of implementing these two features are reduced to the cost of the components themselves. This doesn't entail large design - or financial costs compared with the VR. Considering the great benefits to be had from a chopper and HBDS circuit these should be a natural part of the system containing the VR for excitation systems.

VIII. Conclusion and final recommendations

Simulations and the excessive literature on the VR for other applications suggest that the VR is a viable option for exciter-purposes in the scope of both RPE and static excitation. The main challenge is the large input-inductance arising from the feeder. This can be overcome by changing the winding-configuration, possible with simply using PWM rather than hysteresis-control.
The VR is at the time being a more costly alternative in RPE and excitation-systems and entails more maintenance. But the expected lifetime of components and cost as a portion of the whole machine is so low that this pose no greater drawback for the VR compared to other topologies.

A. Additional circuitry

To enhance the VRs operation and dynamic response a chopper should be added on the output. To ensure rapid demagnetization the HBDS-system should also be implemented, although less pressing than adding the chopper.

B. Implementation in Svante testrig

Before building a custom VR for the testrig, a commercial version should be bought and tested. The only commercial available VR that the author is aware of is provided by Texas instruments [20] and has somewhat lower current-ratings than what is needed at Svante. Furthermore one should build a custom VR designed for the testrig. Film-capacitors and press-packed IGBTs should be used.

As with the mechanical issues regarding RPE, earlier research and technology indicates that this should pose no problem for implementation. Nonetheless is should be implemented in Svante as a proof-of-concept.

C. Further research

A comparative study between the VR, the one-switch VR and six-switch boost converter for this application should be conducted. Simulation, also including chopper on the output if necessary, would give a picture of the suitability of the different topologies. Field forcing and rapid-demagnetization should be a part of the requirements. As in this thesis the problem where the input-inductance is given, rather than being a degree of freedom, should be solved.

Power capacitors, IGBTs, drivers and other necessary components should be tested under the rotary forces they will experience being mounted on the rotor of a typical synchronous generator. Even thought earlier research strongly indicates this won't cause any damage to the components, a thorough test in the exact mechanical stress-situations should be conducted. This study is advised to find inspiration, and possibly initiate a collaborations with, the authors of the work that have been done at Sintef regarding aquatic pressure applied to similar components. A model of expected lifetime for the components should be produced to get an general idea of the need for maintenance and control.

A prototype rated excitation-systems should be built. Chopper and HBDS should be integrated in this prototype, but the prototype should be constructed in such manner that C_{link} and L_s may be easily exchanged to study the effects of different L_s. PWM-controlled should be explored after a successful implementation of hysteresis-control. In addition to the exhaustive literature on the subject which is in part mentioned in the references to this thesis, inspiration should be drawn from the documentation of the VR offered by Texas Instruments.

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IX. Appendix

A. Boards
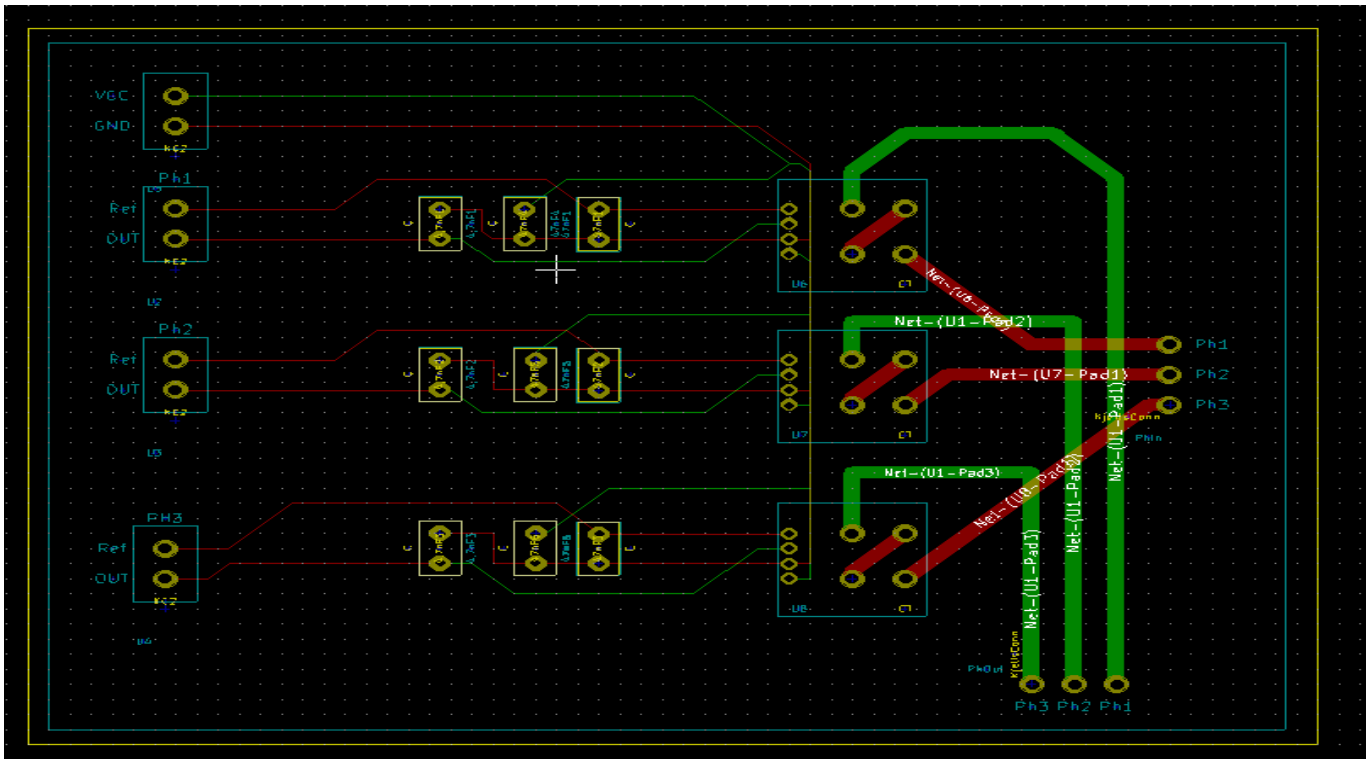
Fig. 74. Board layout for the three-phase current transducer using the LM25.
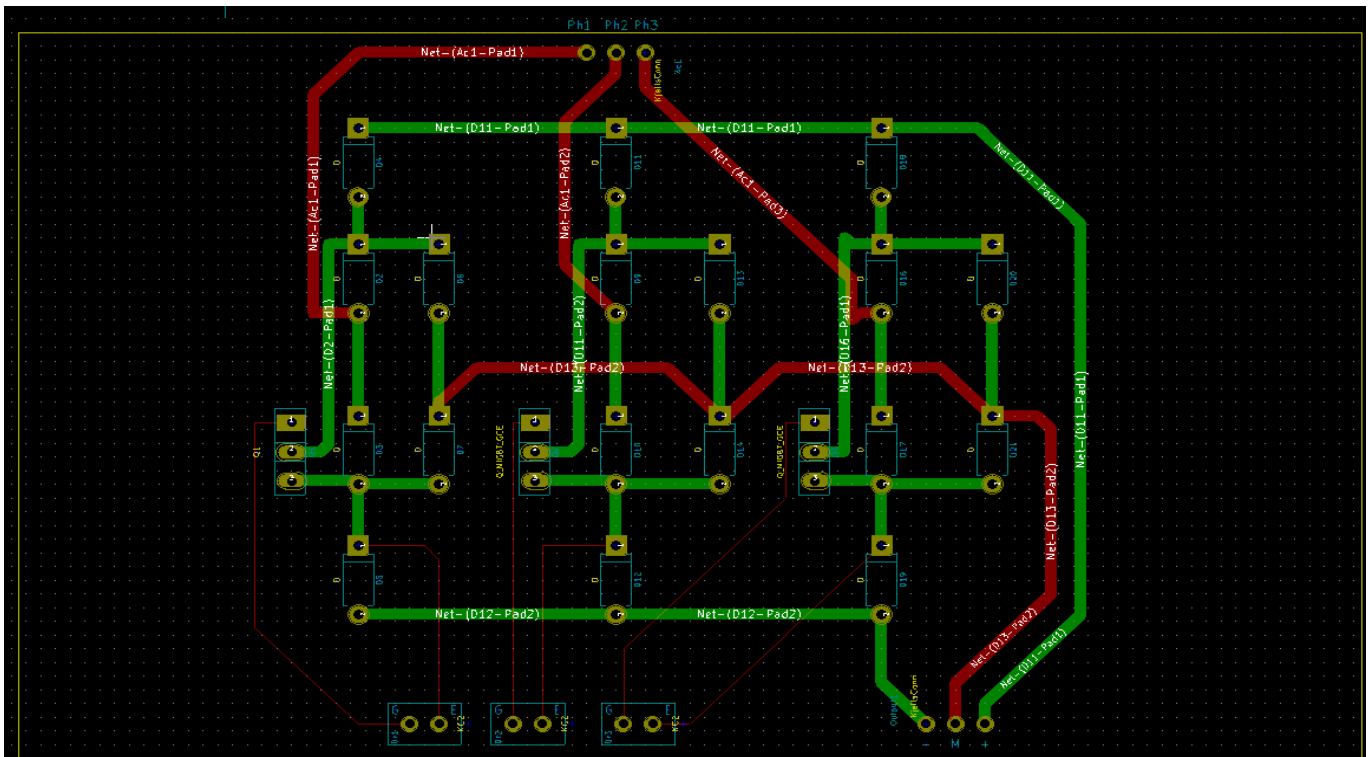
Fig. 75. Board layout for the stripped (caps and inductors externally attached) Vienna
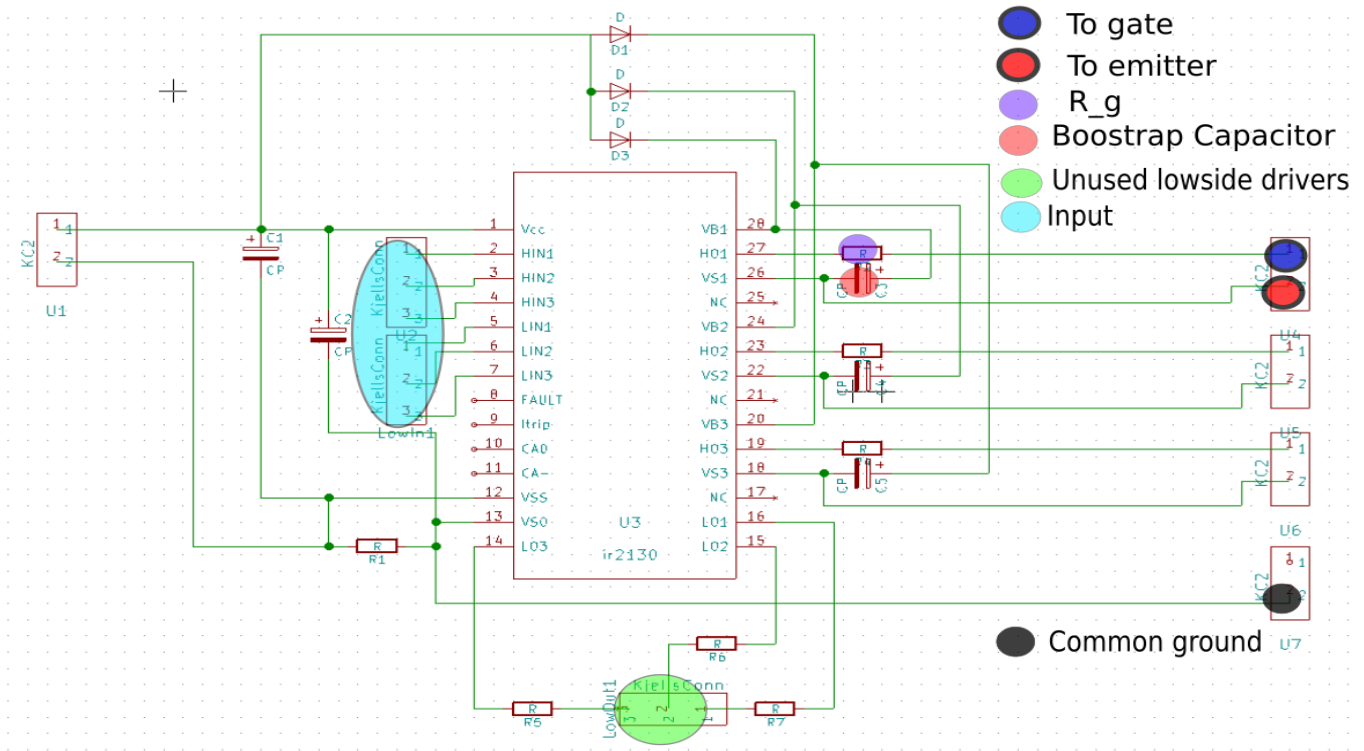
Fig. 76. Schematic of the driver-PCB using bootstrap-configuration. The most notable components are highlighted and explained. In addition to the issue regarding charging of the bootstrap-capacitor, there is also problems with the common ground that needs to be connected into the VR.

B. Simulink - models

1) Vienna-rectifiers:
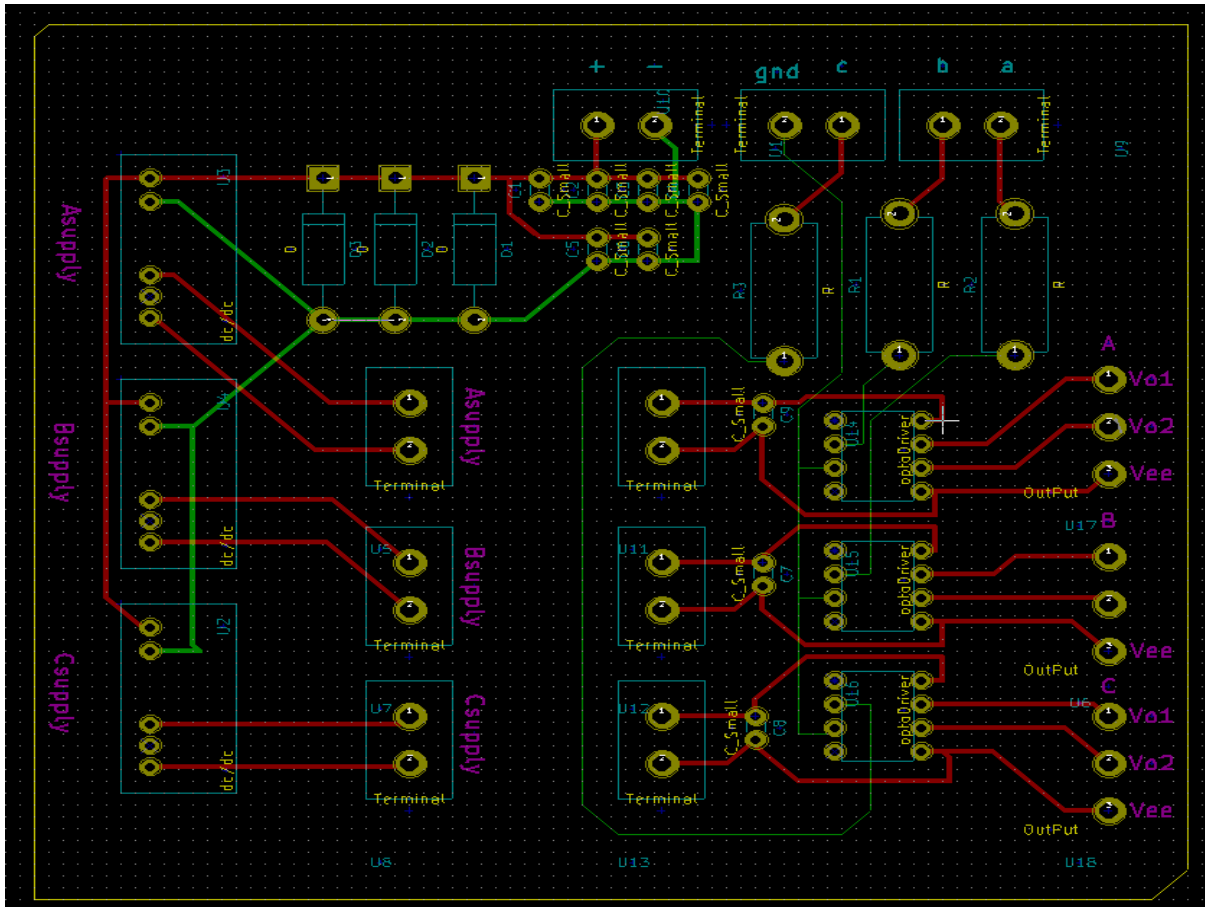
Fig. 77. Schematic of the driver-PCB utilizing optocouplers and isolated voltage-supplies. On the left of the PCB is the dc-dc converters placed, the diodes and capacitors are part of a surge-protection circuit recommended in the application note. The resistors on the input of the optocouplers are current-protection for the internal diodes.
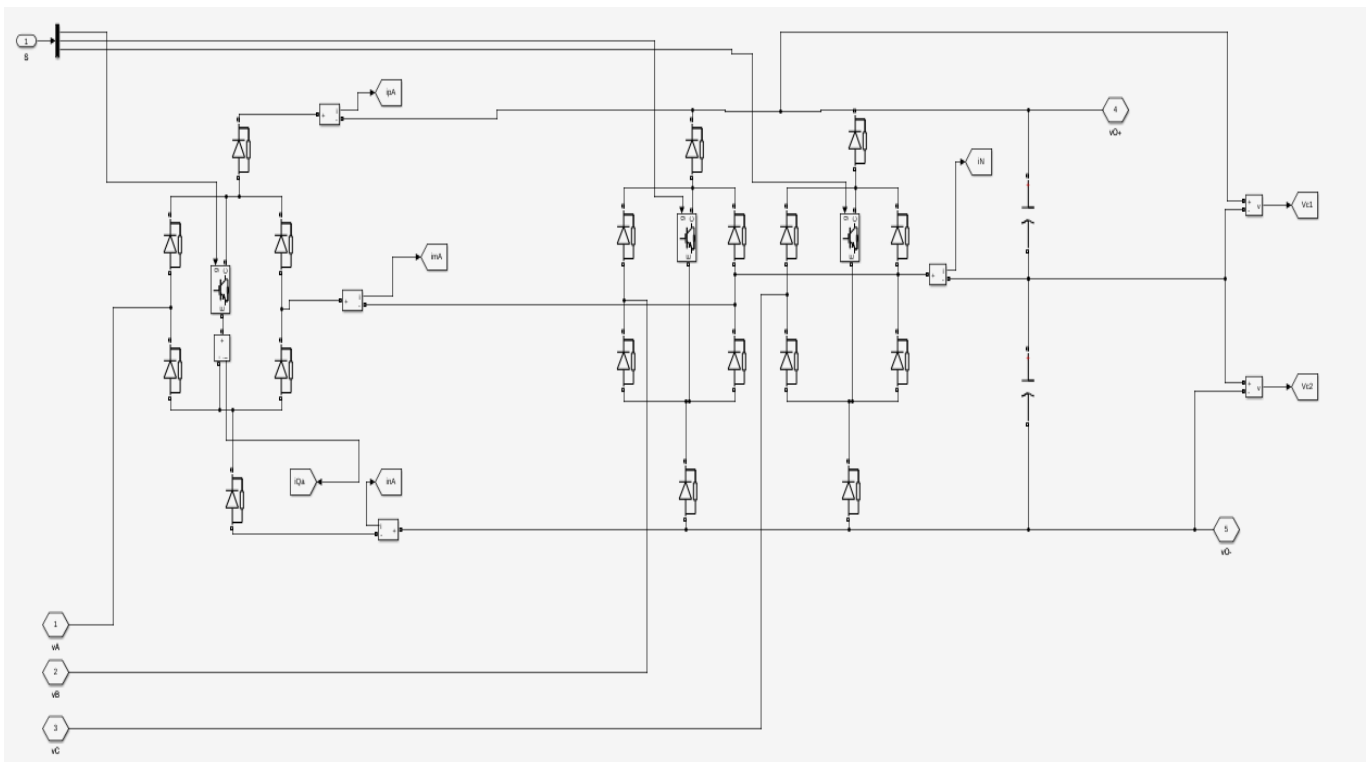
Fig. 78. The more complex modell of the Vienna-rectifier used in building of the demonstration set-up
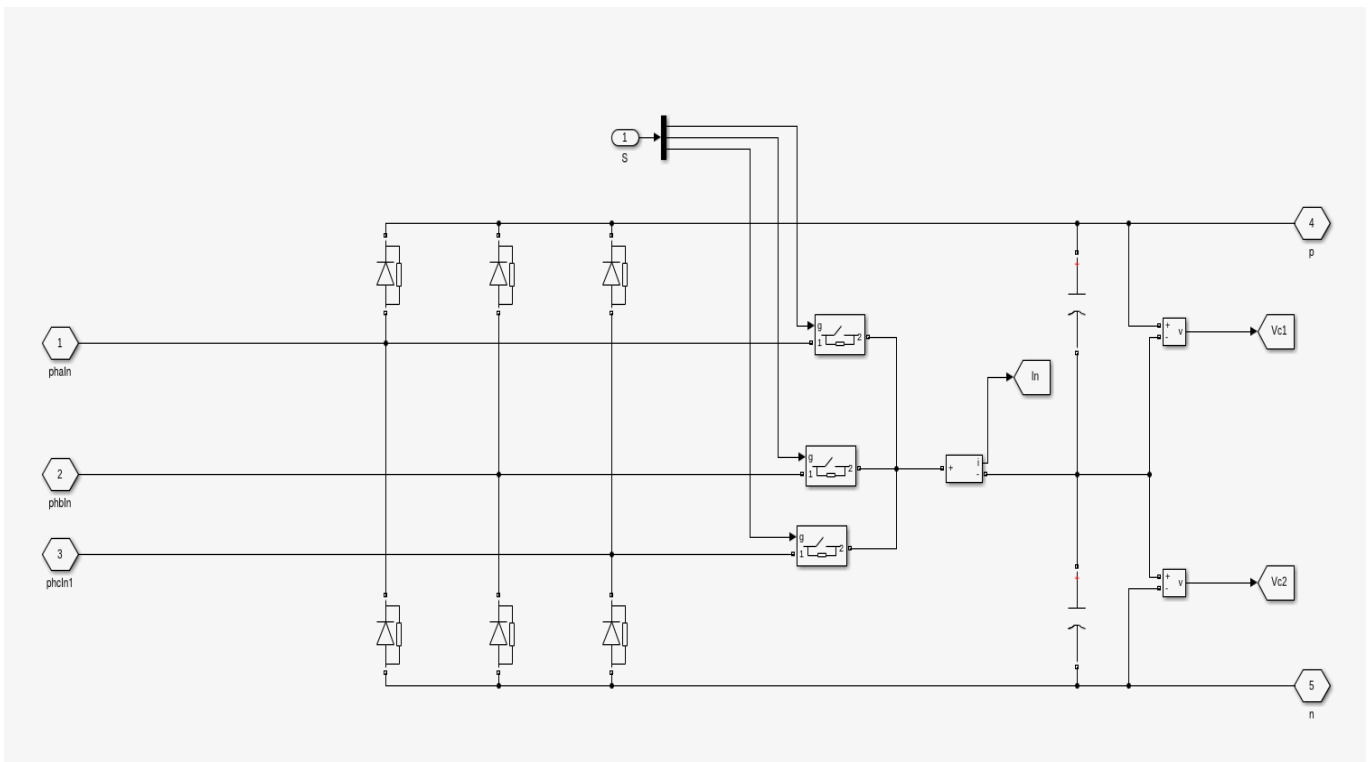
Fig. 79. The simplified Vienna used in the simulation shown in section V
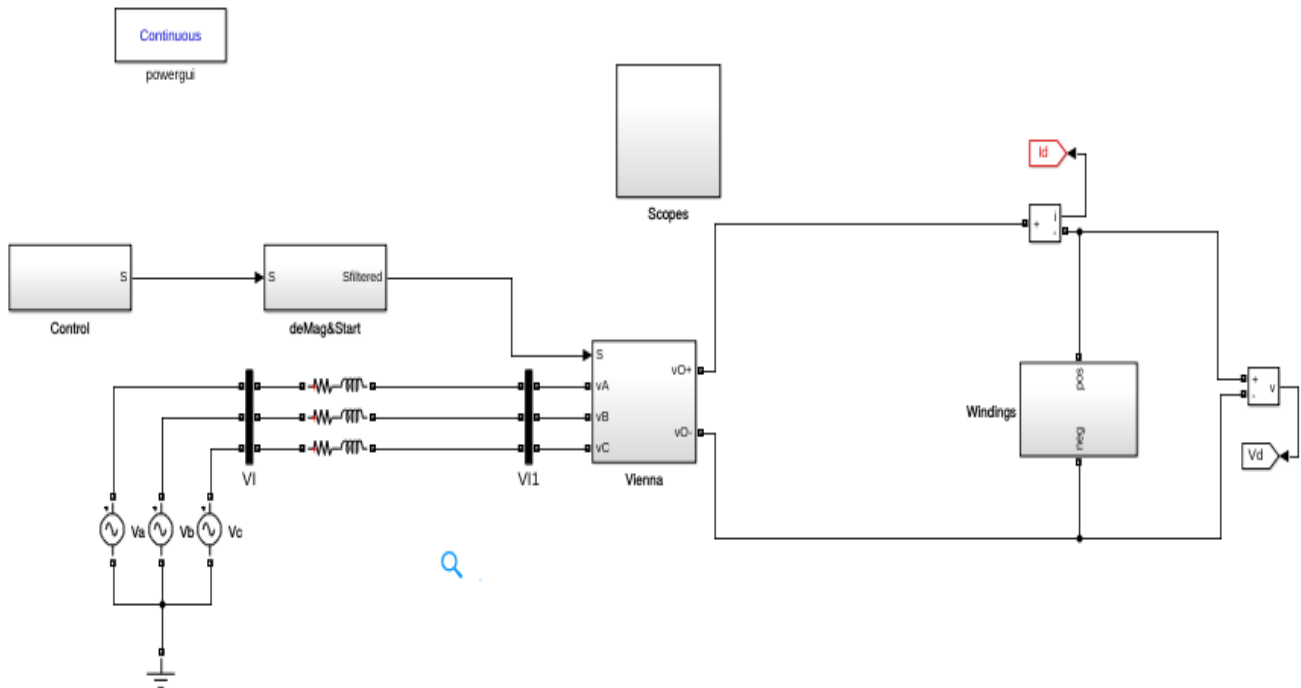
Fig. 80. Modeling the supply as stiff voltage-sources.
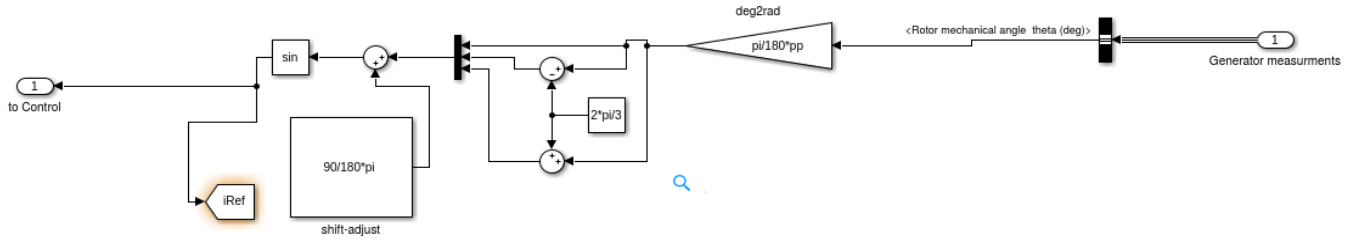
Fig. 81. Deriving the fundamental waveform of u_s from Θ_s. Note that the number of pole-pairs (pp) is included in the calculations. The "shift-adjust" is necessary since the axis of the rotor in the Simulink block is not aligned with phase A, but lies 90 electrical degrees behind.
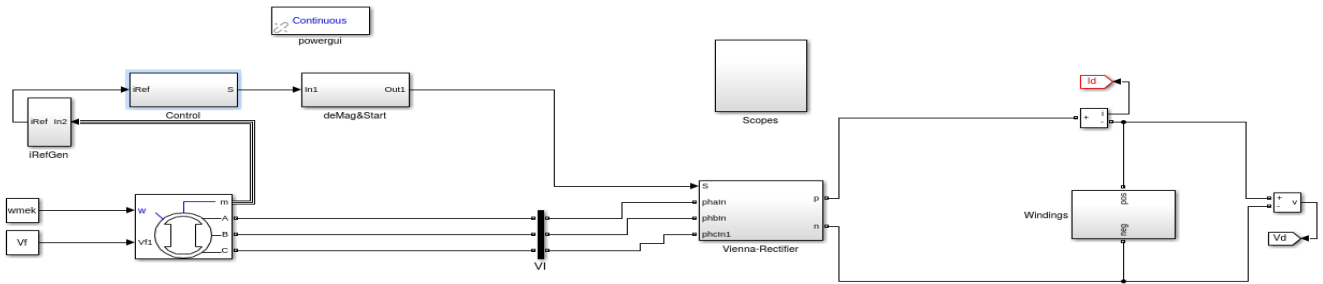
Fig. 82. Using the mechanical block of p.u. synchronous generator to emulating an industrial feeder.
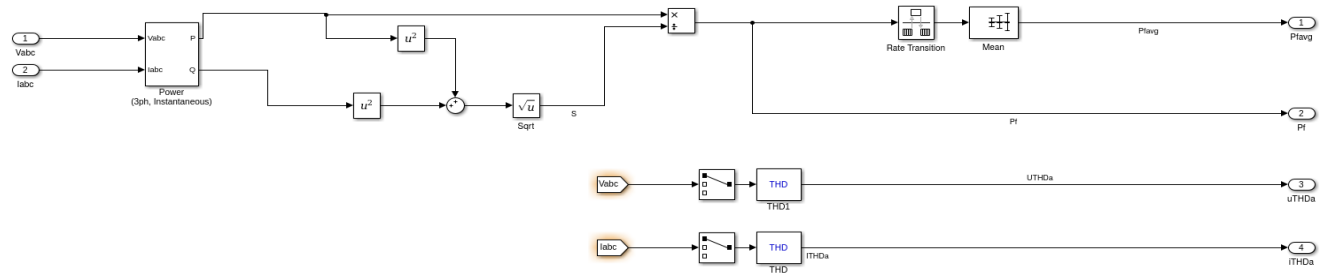
Fig. 83. Using the default blocks to derive the power factor. Note the rate-transition block that is necessary to compute the running mean of the power factor. This is quite heavy on the simulation, and should not be used unnecessary
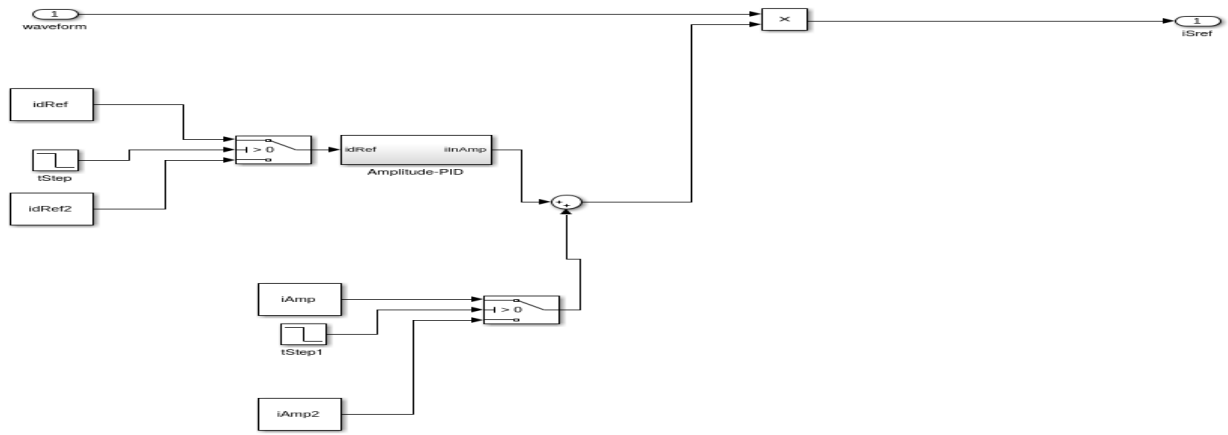
Fig. 84. "iAmp" refers to the offset calculated with eq 44. A step is initiated at tStep, which also corresponds to a change in shift in both "idRef" and offset-value. The input waveform is the one derived from the rotor-position.
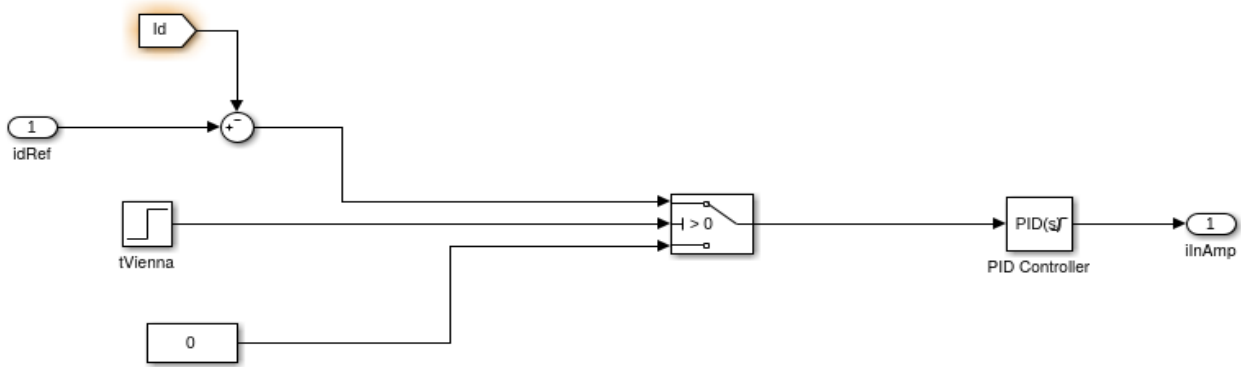
Fig. 85. The default PID-controller also includes anti-windup configuration to prevent the integrator to go too large magnitudes during transient startup. The PID-controller receives zero-error up to the point where the Vienna is turned on "tVienna" to ease simulation.
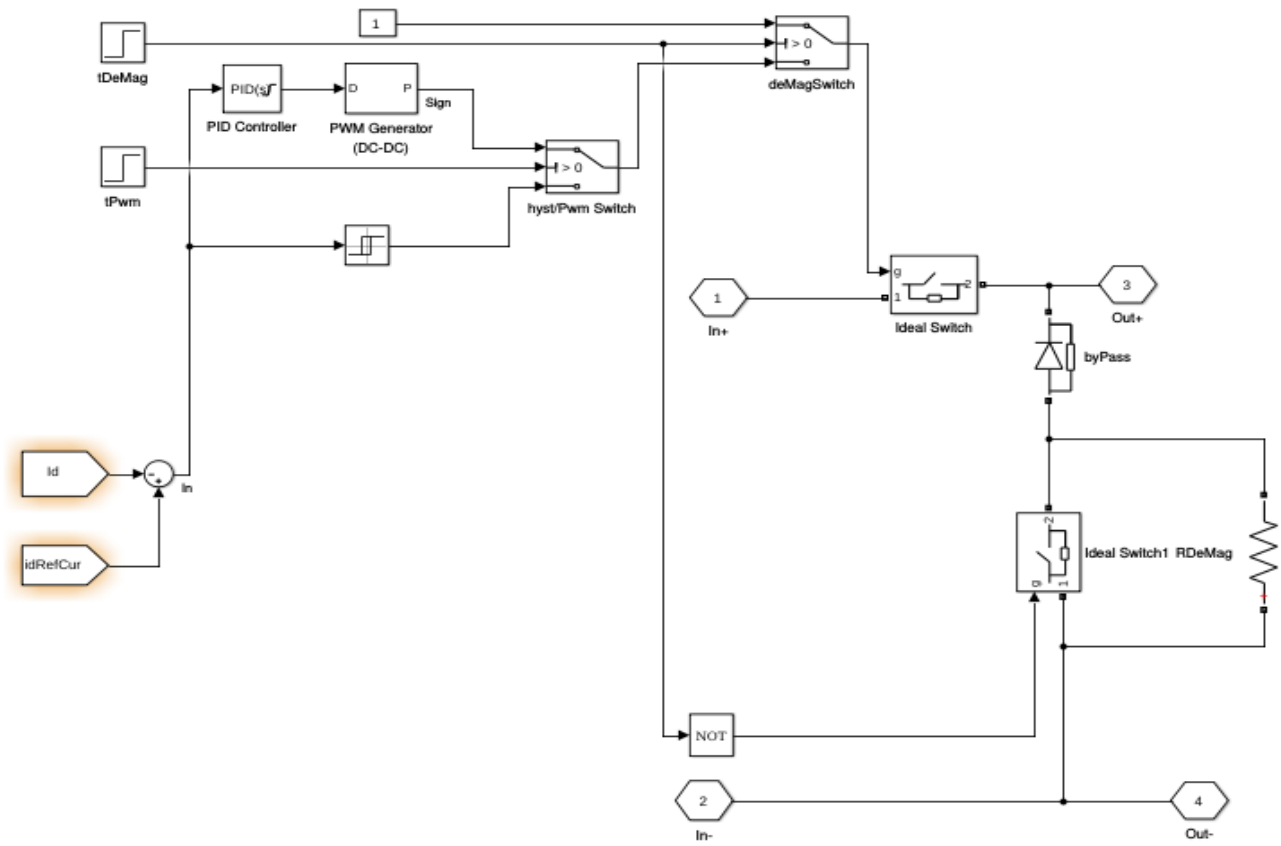
Fig. 86. The chopper configuration with signal routing switching from hysteresis to PWM-control to demagnetization according to stepping-signals.
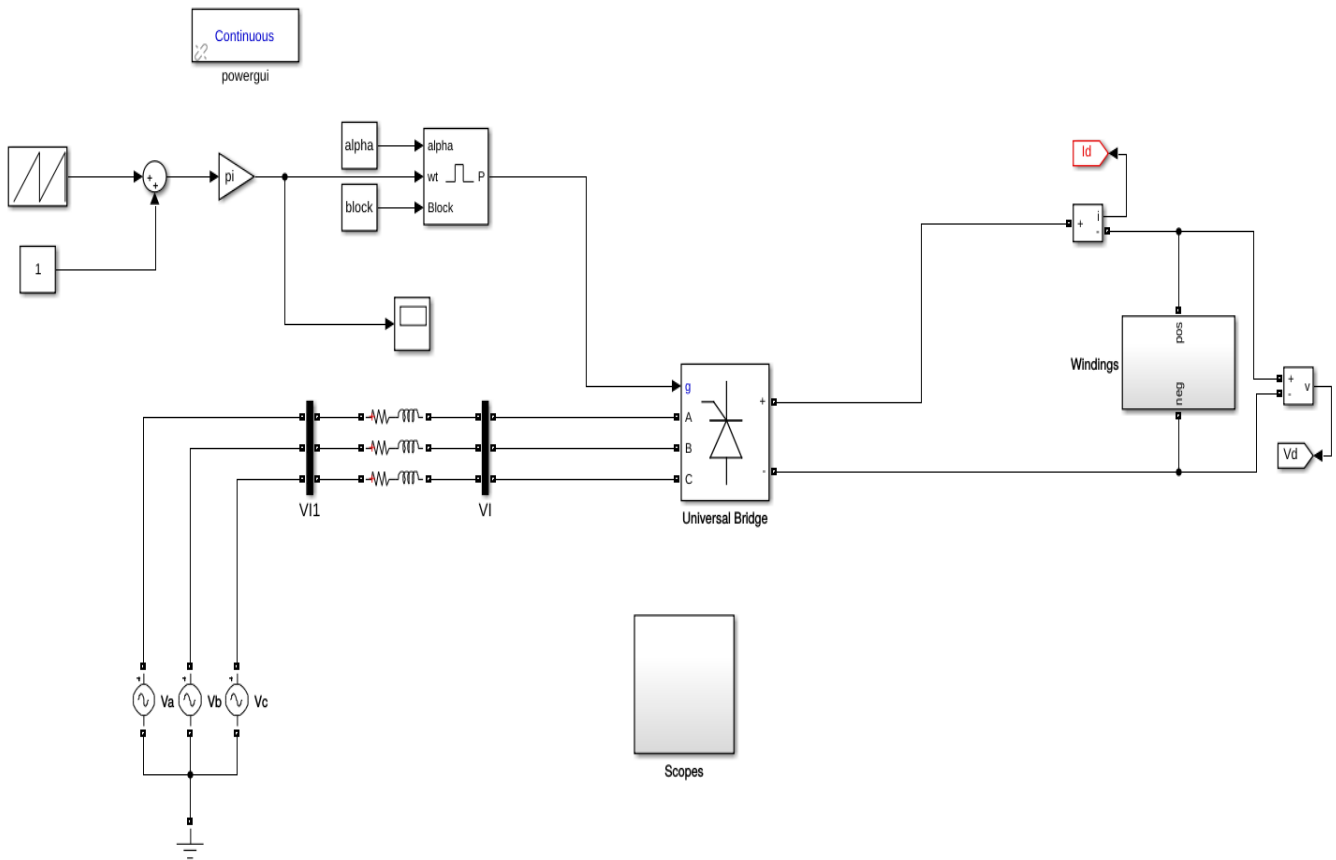
Fig. 87. Implementing a thyristor bridge in Matlab Simulink can easily be done by using included blocks. Since ideal voltage sources are used a sawtooth-signal with some small mathematical operations are used instead of a PLL to speed up simulation.

C. LabView implementation
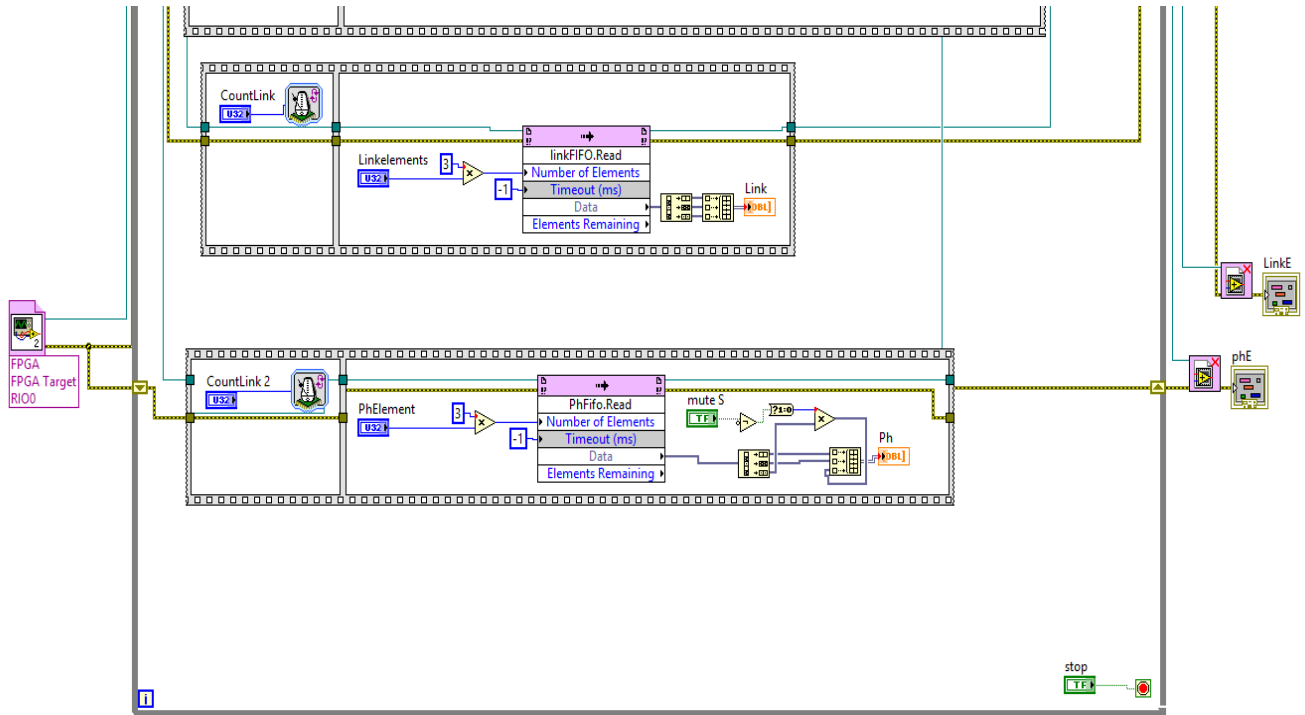
Fig. 88. A portion of the first reading-block on the processor. Here, several signals were shown for three phases. Currents, voltages and switching-signals. In this picture only the dc-link and one phase reading is shown. Note the "mute S" variable. This is to give a clearer view of the currents versus the voltages, without also seeing the switching in the same diagram.
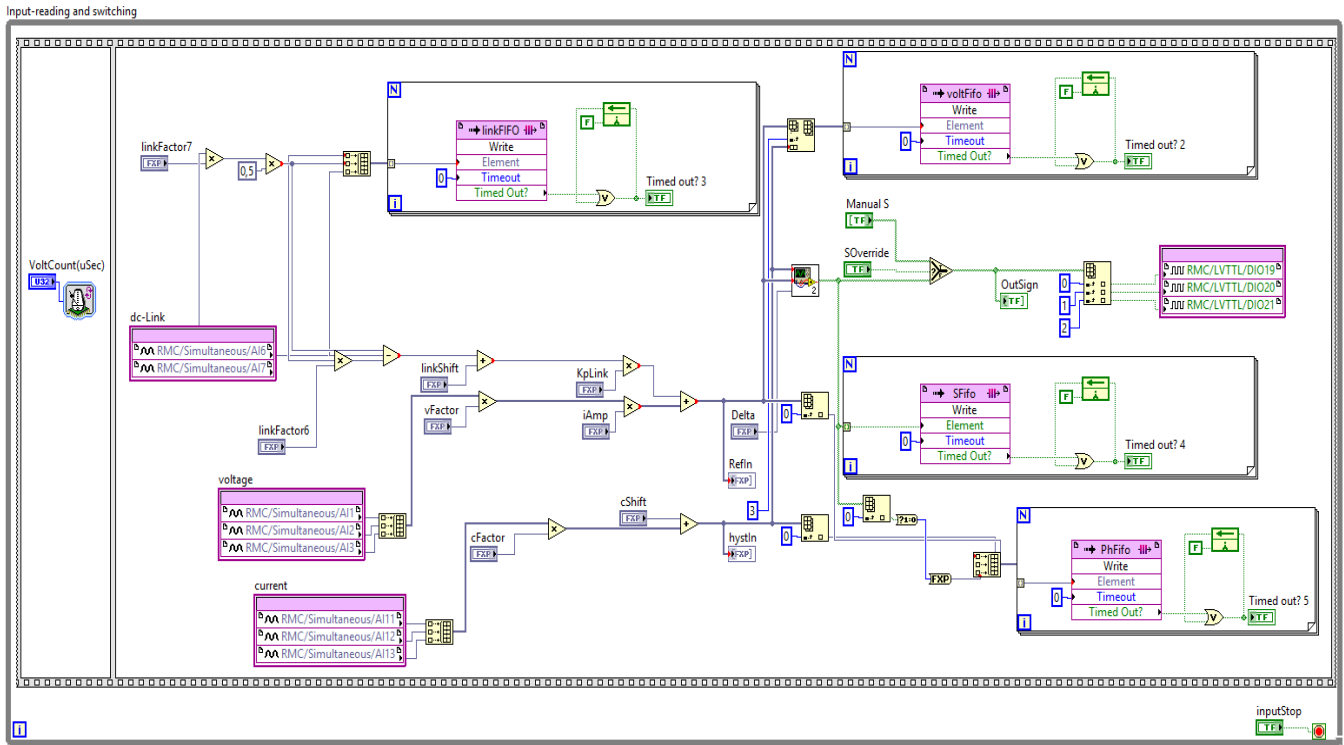
Fig. 89. The initial loop for reading values and writing **S** from the FPGA. Note that the sub-VI is refering to the three phase hysteresis controlblock shown in fig. **??**. The four for-loops are identical. Note the scaling that all the analogue readings experiences. Reading all signals for all phases were off small use during development, so after initial testing the loops were changed to just containing a single phase, the dc-link voltages and the chopper (output). The latter were read in it's own loop, seen in fig. **??**.
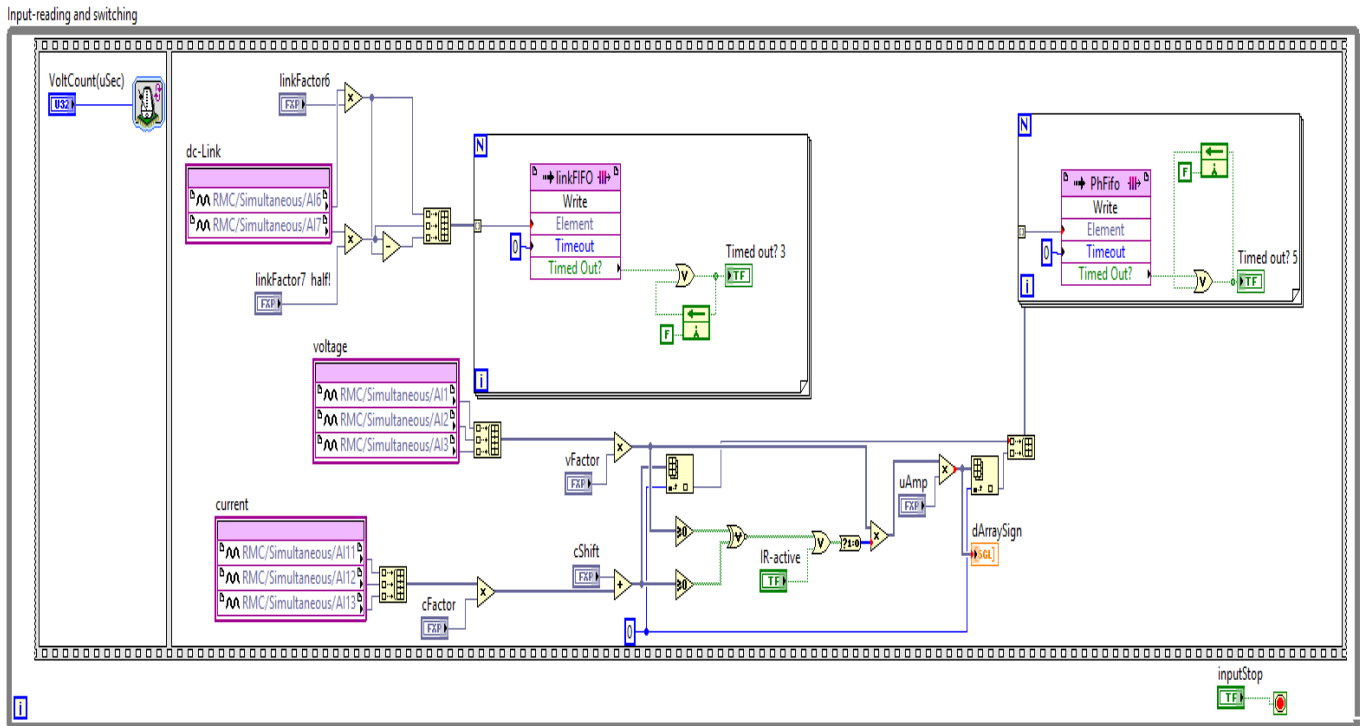
Fig. 90. The reading-loop of the PWM-control. Regarding scaling etc. it is similar to that of hystereis-control. However, note the variable "uAmp" that describes the amplitude of the reference sine-signal of duty-cycles. This is passed to a global variabel dArraySign that is passed to another loop that effectuates this command.
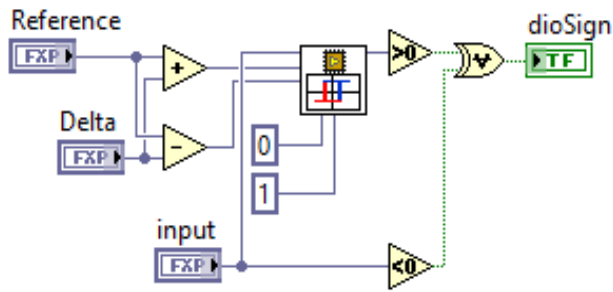
Fig. 91. The hysteresis-controlled, including the modification of eq. (43). The built in hysteresis-block for FPGA is used. An NXNOR block is used to modify for input-sign. The variable dioSign is the output of the control.
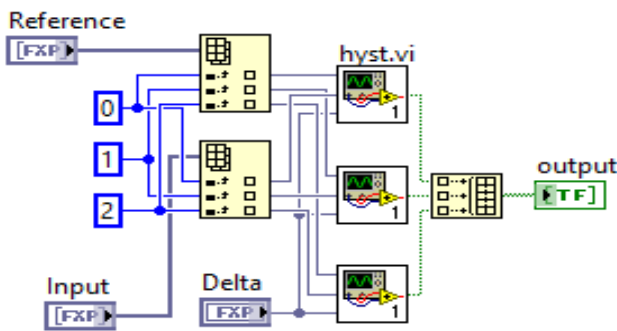

Fig. 92. A three-phase version of the above schematic, dealing with arrays rather than single elements.
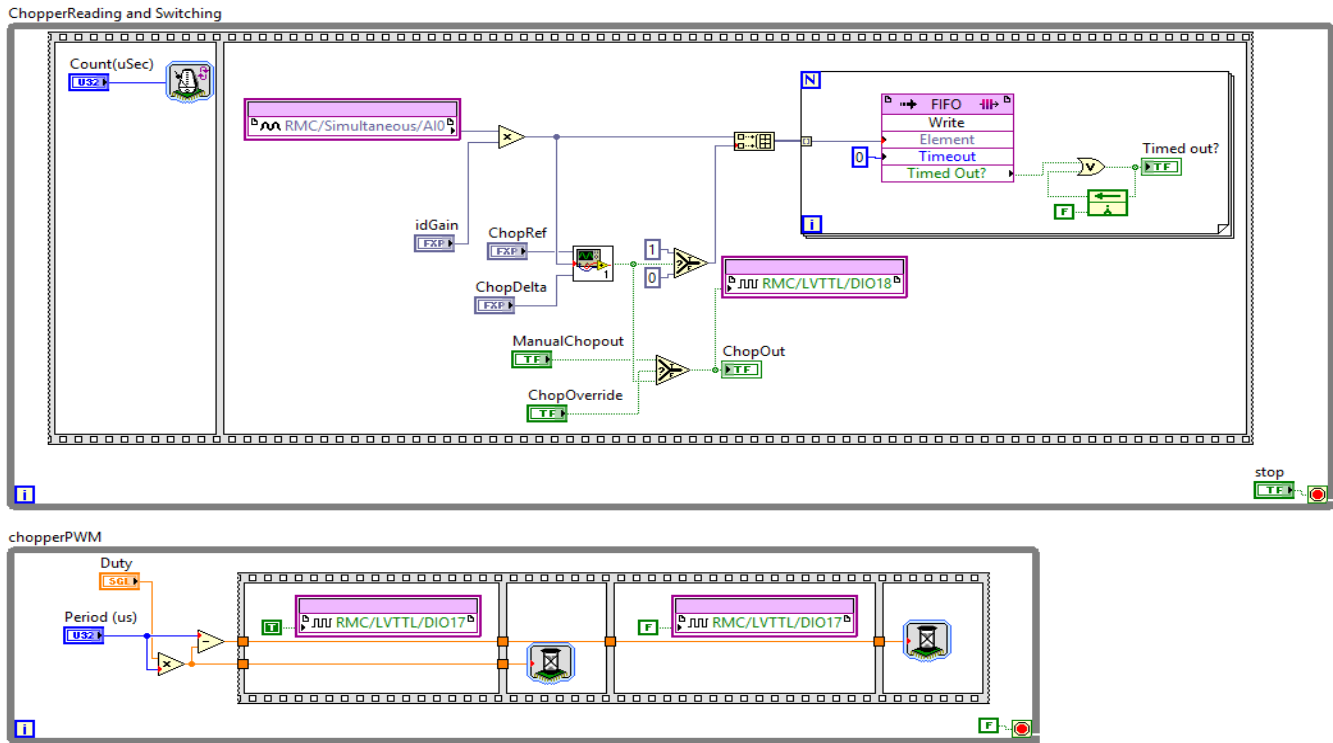
Fig. 93. Here two different alternatives for control for the chopper on the output are shown, hysteresis (upper) and pwm (lower). Note the override-possibility in the upper while-loop. This was very useful during testing. The choice-block in the middle converting a boolean value switching the output to FXP-datatype were necessary to have an array of same datatype passed to the FIFO. The lower implementation is quite straight-forward: A period and a duty cycle is given, resulting in a given wait-period between the designated LVTTL-pin out turning on and off.
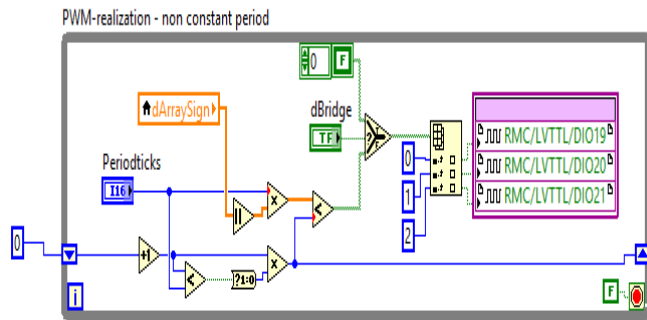
Fig. 94. This is the initial PWM-implementation. It is suspected it was to slow. Another large drawback is that the period is not controllable. Note the overwrite option turning off the VR and making the circuit become a diode bridge.
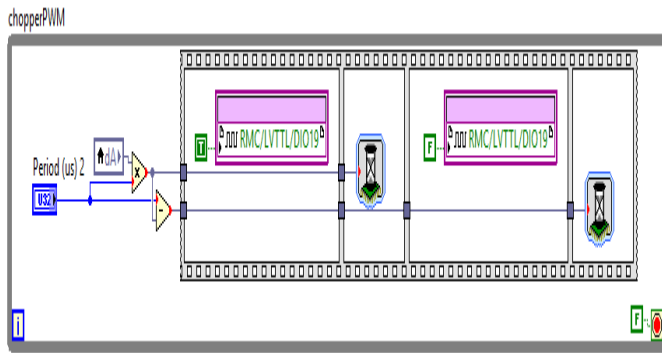
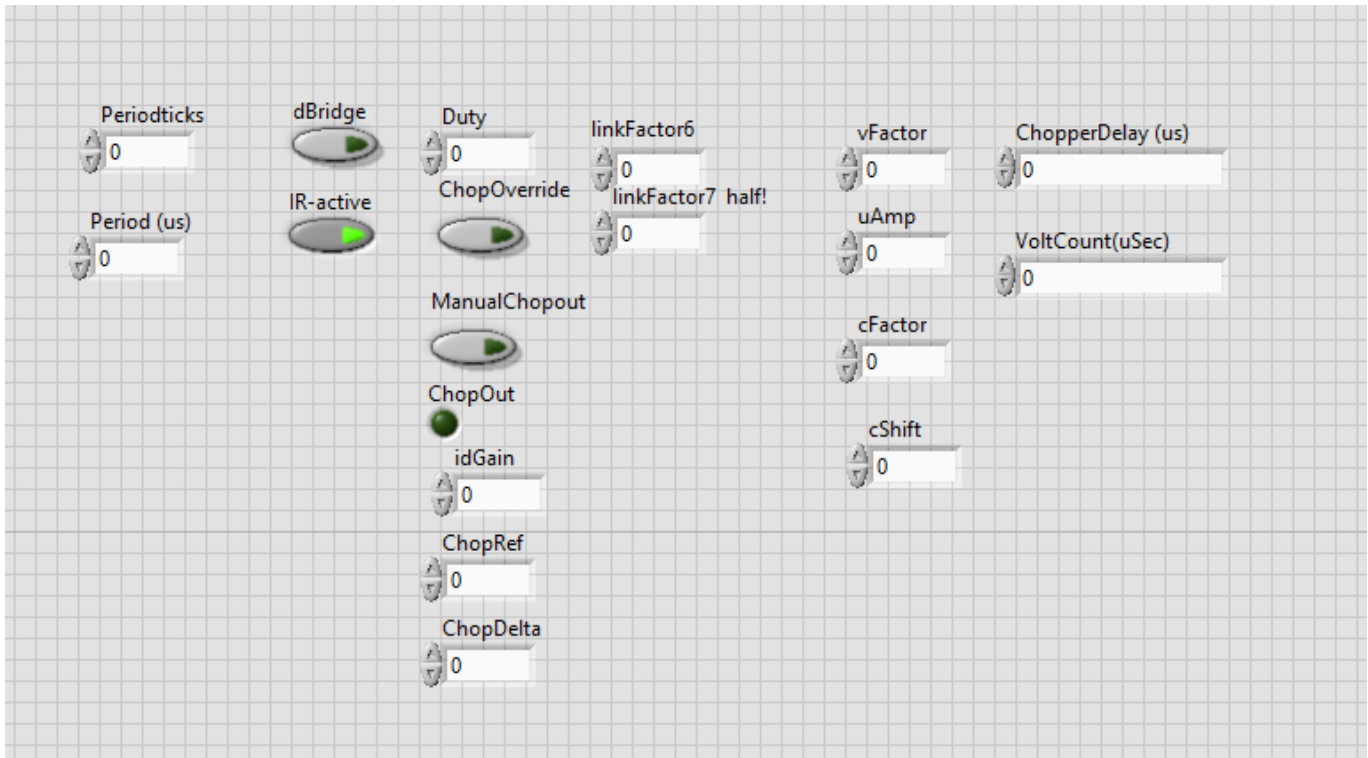Fig. 95. A per-phase PWM-implementation where the period is controllable.

Fig. 96. The control panel of the circuit in the PWM-control. The one of hysteresis-control doesn't differ much, so it isn't shown here. Note that all scalings can be set manually, the IR and whole VR can be turned on/off as well as overriding the chopper is an option.