Monolithic Thin-Film Chalcogenide-Silicon Tandem Solar Cells Enabled by a Diffusion Barrier

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Abstract

Following the recent success of monolithically integrated two-terminal Perovskite/Si tandem solar cells, a lot of interest has been raised in searching for alternative wide bandgap top cell materials with prospects of a fully earth-abundant, stable and efficient tandem solar cell. Thin film chalcogenides (TFCs) such as the kesterite Cu_2ZnSnS_4 (CZTS) could be suitable alternatives. However, unlike Perovskites, TFCs have the disadvantage that generally at least one high temperature step (> 500 °C) is needed during the synthesis, which could damage or contaminate the bottom Si structures. Here, we systematically investigate the monolithic integration of CZTS on a full Si bottom solar cell. As bottom cell, a thermally resilient double-side Tunnel Oxide Passivated Contact (TOPCon) structure is used, with a thin (< 25 nm) TiN layer at the interface between the top and the bottom cells, serving both as diffusion barrier and recombination layer. We show that TiN successfully mitigates the in-diffusion of CZTS elements into the c-Si bulk during the high temperature sulfurization process, and find no evidence of electrically active deep defects in c-Si bulk in samples protected by only 10 nm TiN. Moreover, post-process minority carrier lifetime in Si exceeds 1.5 ms, corresponding to a promising implied V_{oc} (i-V_{oc}) of 710 mV for the Si bottom cell even after the high temperature step. Based on these results, we demonstrate a first proof-of-concept two-terminal CZTS/Si tandem device with an efficiency of 1.1% and a V_{oc} of 900 mV, a value higher than that of each respective reference cell individually. A general implication of this study is that the growth of complex semiconductors on Si using high temperature steps is not technically unfeasible, and can potentially lead to efficient monolithically integrated two-terminal tandem solar cells.

Keywords: Tandem, Monolithic, Two-terminal, Silicon, TOPCon, Calcolgenide, CZTS, CIGS, Passivating Contacts, Diffusion barrier, TiN, Solar cell, Photovoltaic.

1 Introduction

The current global uptake of photovoltaic (PV)-based solar energy has been enabled by the remarkable developments in crystalline Silicon (c-Si) solar cell technologies, both in terms of module efficiencies and costs, with market shares consistently around 90% for decades – a figure which is expected to remain unchanged in the near future [1]–[3]. However, as the Si cell efficiency approaches the Shockley-Queisser (SQ) single-junction limit [4], further cell improvements are now only incremental, and the focus is instead on systems cost reduction and raw material utilization [2], [3].

Multi-junction solar cells can achieve higher efficiencies than the single-junction SQ limit, with AM 1.5 limits of around 45% and 50.5% for double (also called tandem) and triple-junction solar cells, respectively [5], [6]. However, to transition the global PV market from a single- to a multi-junction solar cell technology, the following conditions must be met: 1) The efficiency gains should not sacrifice cost competitiveness; 2) The raw materials used should be abundant, inexpensive and non-toxic; 3) Each individual junction must be stable and have a lifetime of decades.

Various multi-junction cell configurations have been proposed and demonstrated experimentally, particularly with Si and III-V semiconductors, reaching efficiencies of 32.8% and 37.9% for tandem and triple-junction cells, respectively [7]–[10]. In space applications, multi-junction III-V solar cells have been used almost exclusively since the late 1990s, but with costs not competitive with the single-junction c-Si technology [11], [12]. Out of all the possible multi-junction configurations, a monolithically integrated two-terminal (MI-2T) tandem device is considered *a priori* to be the most feasible for cost-competitive, large-scale applications, as it retains the module design simplicity of single-junction technologies and minimizes the total number of processing steps. Despite all its potential advantages, MI-2T tandem devices are challenging to achieve in practice because every processing step has to be compatible and the properties of the preceding interface and layers should not deteriorated [13].

For the same reasons that gave it a dominant position in the PV market, c-Si is an excellent partner for a tandem solar cell. Its bandgap of 1.12 eV is near ideal for a MI-2T tandem – when used together with an absorber with a bandgap of 1.72 eV, a theoretical maximum efficiency of close to 43% can be achieved [6], [7]. Recently, a lot of interest has been raised after a series of MI-2T Perovskite/Si tandem devices achieved efficiencies over 25%, with the current record set at 28% [14]–[16], a value higher than that of the best Si solar cell.

Thin film chalcogenides (TFCs) such as CdTe, $CuIn_xGa_{1-x}S_ySe_{1-y}$ (CIGSSe), $Cu_2ZnSnS_xSe_{1-x}$ (CZTSSe) and their respective solid solutions and cationic substitutions could be suitable alternatives to Perovskites due to their increasing single-junction solar cell efficiencies, competitive production costs and superior stability. Indeed, a 16.8% $Cd_{1-x}Zn_xTe$/Si tandem cell has been demonstrated using low temperature molecular beam epitaxy (MBE) [17]. However, in most cases, TFCs have the disadvantage that a high temperature step (>500 ℃) is needed, compared to Perovskites which can be processed at low temperatures (<200 ℃) [13], [14]. To the best of our knowledge, the implications of high temperature processing on the feasibility of a MI-2T TFC/Si tandem device remain relatively unknown and have not been directly assessed experimentally.

In this work, we discuss the challenges of producing TFC/Si MI-2T tandem devices, using the sulfide kesterite Cu_2ZnSnS_4 (CZTS), an earth abundant and environmentally friendly representative of the TFC group. In particular, we assess the contamination and degradation of a Tunnel Oxide Passivated Contact (TOPCon) Si bottom cell during the CZTS processing steps. We test the introduction of a thin titanium nitride (TiN) diffusion barrier layer between the Si and CZTS structures and use the results to evaluate the process compatibility between CZTS and Si. We show that this compatibility can be achieved, and report on a first proof of concept CZTS/Si tandem solar cell with an efficiency of 0.5% and a V_{oc} near 800 mV, a value higher than that of each respective reference cell individually. Moreover, we suggest strategies for future device improvement.

1.1 The Top Cell: CZTS

The kesterite sulfide-selenide CZTSSe raised interest as an all earth abundant alternative to CIGSSe consisting of non-toxic elements (in particular the sulfide CZTS), achieving solar cell efficiencies above 10% using similar industrially upscalable methods such as sputtering [18]. Sulfide CZTS, in particular, has some features which suggest that it could be a promising tandem partner for Si. Through different solid solutions and cationic substitutions, the bandgap of kesterites can be tuned – for instance, through Ge or Ag incorporation the bandgap of sulfide CZTS can be increased from the nominal 1.5 eV to about 2.1 eV, an ideal range for tandem applications [19]–[24]. Moreover, CZTS and Si are closely lattice-matched, with an a-axis lattice mismatch of less than ±0.1%, as compiled for example in [25], [26]. This means that heteroepitaxial growth of CZTS on Si should be possible, and this has indeed been proven experimentally [27]–[29]. While this allows in principle for epitaxially growing CZTS/Si tandem devices (free of grain boundaries), epitaxial growth of CZTS on Si with the necessary tunnel junction structures has not been demonstrated to that extent yet.

So far, the TFC solar cells with the highest efficiencies, in particular in the case of CZTS, involved at least one high temperature step [26] (with the notable exceptions of MBE [17] and monograin technology [30]). Herein, we argue that one of the biggest challenges towards a TFC/Si MI-2T tandem device could be a cross-contamination of the bottom Si cell

with metallic elements such as Cu or chalcogens like S, during the high temperature step.

1.2 The Bottom Silicon Cell: Tunnel Oxide Passivating Contacts (TOPCon)

The tunnel oxide passivating contacts (TOPCon) structure has played a key role in the recent efficiency improvements of silicon solar cells [31]–[35]. The structure consists of a stack of thin (~1.2-1.5 nm) SiO_2 layer underneath a highly doped (Phosphorous or Boron) polycrystalline silicon layer (polySi) at each side of a crystalline silicon (c-Si) wafer, which provides excellent surface passivation and carrier selectivity. Consequently, a high implied V_{oc} of 750 mV and an external V_{oc} of up to 739 mV have been achieved [36]. In contrast to its aSi:H heterojunction counterpart, the TOPCon structure alone is resilient to high temperature annealing up to 900 ºC, which is well above the typical annealing temperatures used in the synthesis of chalcogenide semiconductors and other front and backend processes. Moreover, the simple one-dimensional current transport and full coverage of contacts at both sides allows for very low contact resistivity and thereby low FF losses [37]. A major drawback of using a front polySi contact in a single-junction device is the parasitic absorption losses within the polySi layer in the blue wavelength region. As a result, a J_{sc} loss of 0.5 mA/cm^2 is expected for every 10 nm of polySi [38]. However, this is not a limitation for a tandem configuration, where the high-energy photons are absorbed in the top cell. Thus, the double-sided TOPCon structure can be an ideal candidate for double-junction tandem solar cell.

1.3 The need of a diffusion barrier layer

When a nearly complete silicon solar cell is used as substrate for the growth of a TFC, there is a risk of contamination from metallic and chalcogen elements that should be thoroughly assessed. In this contribution, we study the example of co-sputtered CZTS precursors from Cu, ZnS and SnS targets. During co-sputtering, the impinging energetic ions and neutrals can directly cause sputter damage, or contaminate the Si bulk by implantation. After co-sputtering, CZTS is formed by a high temperature reactive annealing in a sulfur atmosphere. Here, the elements Cu, Zn, Sn and S (the latter both in the precursors and in the atmosphere) can diffuse into the Si bulk. We note that this high temperature step is of particular interest, as it is nearly ubiquitous in high-quality TFC fabrication, even in single-step processes (for instance co-evaporation of CIGS).

Copper contamination in silicon deserves special consideration as it is a common element of both the CIGS and the CZTS group of alloys and, most importantly, because it is one of the most common detrimental contaminants known in crystalline Si, as widely reported in the photovoltaic and integrated circuit industries [39]–[41]. Copper has a high diffusivity in Si, and can diffuse through the entire thickness of a Si wafer at room temperature in a matter of hours, although the solid solubility is $< 10^{15}$ cm^{-3} at the relevant temperatures [39]. Cu exhibits a complex defect physics in Si, leading to point defects and complexes, decoration of extended defects, precipitation of copper silicides, out-diffusion to the surface and segregation phenomena. In particular, copper silicides have been shown to lead to a mid-gap defect band in Si and a high recombination activity [42], detrimental in solar cells.

Although studied to a lesser extent than copper, the other elements of CZTS could also be harmful contaminants for a bottom Si cell. Zinc can introduce near-midgap defect levels in Si as shown by pure diffusion studies [43]–[45]. Tin was studied in particular as a dopant to improve the radiation resistance of c-Si devices, but was also found to form midgap states in Si [46], [47]. Finally, sulfur was studied notably in "black silicon" processing, where it was found that its incorporation creates deep bandgap states, which increase the infrared light absorption in Si, making it appear more "black" [43], [48], [49].

Here, we suggest that one possible way to prevent bottom cell contamination is using a diffusion barrier layer at the bottom cell/top cell interface. In general, a barrier layer must have properties such as mechanical stability, providing good adhesion, high temperature stability and low diffusivity for the required elements. For tandem solar cell applications, it must also be electrically conductive and transparent in the near infrared region. To the best of our knowledge, only one published work directly addresses this problem, suggesting the use of ZnS as a barrier layer for the growth of CZTS/Si tandem cells [50]. In this work, we propose titanium nitride (TiN) as a barrier layer at the CZTS/Si interface. TiN has been extensively studied as possible barrier layer for copper metallization in integrated circuits, and although it is arguably not the most effective barrier known against Cu diffusion [41], [51], [52], it has been employed as a back contact modification and barrier against oversulfurization (or overselenization) in single-junction CZTSSe cells, proving to be compatible with devices with up to 9% efficiency [53]–[57]. Due to its poor transparency, the TiN thickness has to be limited to only a few nm.

By contrast, in a MI-2T Perovskite/Si tandem solar cell, a Si-based tunnel junction or a simple interface recombination layer based on a transparent conductive oxide (TCO) can be used to achieve high performing devices [13], [14]. This could also be a possibility if contamination-free growth of TFCs on Si can be proven. In this regard, it is noteworthy to mention that there are studies suggesting that some TCO substrates could be compatible with TFC growth conditions [21], [58].

2 Materials and Methods

A set of double side polished (100) n-type Cz-Si wafers were used, with 100 mm in diameter, 1 Ω.cm resistivity and 350 μm in thickness.

The fabrication process of the TOPCon structure is as follows. After the wafers were cleaned in RCA1 (H_2O_2:NH_4OH:$5H_2O$) and RCA2 (H_2O_2:HCl:$5H_2O$) mixtures, ~1.2 nm of SiO_2 (Tunnel Oxide or TO) was grown by chemical oxidation in a 65 %wt HNO_3 solution at 95 °C. Subsequently, ~40 nm polySi layers were deposited using Low Pressure Chemical Vapor Deposition (LPCVD) at 620 °C, with SiH_4, B_2H_6, and PH_3 as precursors for p+ and n+ polySi layers, respectively. The samples were then annealed in N_2 at 850 °C for 20 min for further dopant diffusion and activation. All the samples have a symmetrical passivation of TO/n+polySi on both sides, except in two cases: for DLTS, this passivating stack was not used, and for the tandem solar cell fabrication, an asymmetrical passivation was used, with TO/n+polySi on the front and TO/p+polySi on the rear side. Additionally, for the fabrication of the tandem cell, a hydrogenation process was performed on the as-passivated bottom cell precursor wafer. In this regard, a sacrificial ~ 75 nm hydrogenated SiN (SiN:H) layer was deposited on both sides of the wafer using Plasma Enhanced Chemical Vapor Deposition (PECVD) at 300 °C. After a hydrogen drive-in process at 400 °C for 30 min in N_2 atmosphere, the SiN:H layers were stripped in a buffered HF solution. The alternative 40 nm passivating Al_2O_3 layer was deposited by Atomic Layer Deposition (ALD) using tetramethylammonia (TMA) and H_2O as precursors.

TiN barrier layers (<25 nm) were deposited in a Picosun Plasma-Enhanced ALD (PEALD) chamber using $TiCl_4$ and NH_3 precursors at 500 °C. A metallic Cu layer with 100 nm was sputtered on the TOPCon structure and annealed at 550 °C in vacuum ($1x10^{-6}$ mbar). CZTS precursors were co-sputtered from Cu, ZnS, and SnS targets, and annealed in a reactive N_2 atmosphere containing 50 mg of S pellets, at dwell temperatures of 525-575 °C for 30 min, in order to form CZTS films with a thickness around 300 nm. This CZTS thickness was chosen based on optical simulations (not shown here) and J_{sc} results from single junction CZTS devices, in order to match the electrical current of the two cells. The Cu, CZTS and TiN layers were removed after the sulfurization/annealing step, in a mixture of H_2O_2:$4H_2SO_4$ (piranha) and RCA1 solutions, followed by a dilute HF dip prior to lifetime, SIMS, and DLTS measurements. For the RBS measurements, only piranha was used.

The effective minority carrier lifetime (τ_{eff}) of Si was measured by the microwave detected photoconductance decay method (μ-PCD) in steady-state configuration and 1-sun illumination using an MDP lifetime scanner from Freiberg Instruments. The reported lifetime values are mapped over the whole wafer area with 1 cm margin from the edges. The i-V_{oc} values were calculated based on the method described in [59].

The in-diffusion depth profile were measured by Secondary Ion Mass Spectrometry (SIMS) and Rutherford Backscattering Spectroscopy (RBS) on selected samples. The SIMS depth profiles were obtained from a Cameca IMS-7f microprobe. A 10 keV O_2^+ primary beam was mainly utilized, and rastered over 150 × 150 μm², and the positive ions were collected from a circular area with a diameter of 33 μm. For sulfur, however, a 5 keV Cs^+ primary beam was employed, and clusters of $^{32}S^{133}Cs$ were detected to minimize matrix effect and avoid mass interference. The quantification of Cu depth profiles was obtained by measuring an implanted reference sample, ensuring a ±10 % error in accuracy. The crater depths were measured by a Dektak 8 stylus profilometer, and a constant sputter rate was assumed for the depth calculation. The RBS measurements were done using 2 MeV He ions and a silicon PIN diode detector under a 168° angle. The collected RBS data was analysed and fitted by a RUMP simulation [60].

Deep level Transient Spectroscopy (DLTS) was used to characterize electrically active defects in the Si bulk. DLTS measurements were performed on circular Schottky diodes (1 mm diameter), where 50 nm thick Pd contacts were deposited by thermal evaporation. The backsides were coated with silver paste to form an ohmic contact. During the measurements the diodes were held at -5 V reverse bias and pulsed to 1 V, filling all majority traps within the depletion width of ~1 μm. The samples were cooled to 35 K by a closed-cycle cryostat and six rate windows (with lengths $2^i \times 10$ ms, i = 1, …, 6), were used to record the capacitance transients while heating to 300 K. The transients were multiplied by a lock-in weighting function for improved signal extraction. Further details on the method and setup are given in [61].

For the monolithic CZTS-Si tandem device, a 50 nm CdS layer was used as the buffer to form the p-n heterojunction of the top cell, followed by a 50 nm intrinsic i-ZnO and a 350 nm Al-doped ZnO (AZO) as the TCO layer. A 500 nm Ag layer was thermally evaporated as the back contact. No front metal contacts were used for simplicity, as the active tandem cell areas were only 3×3 mm². The full tandem solar cell was post-annealed on a hot plate in air at 250 °C for 15 min.

The J-V characteristic curves of the solar cells were measured at near Standard Test Conditions (STC: 1000 W/m², AM 1.5 and 25 °C). A Newport class ABA steady state solar simulator was used. The irradiance was measured with a 2x2 cm² Mono-Si reference cell from ReRa certified at STC by the Nijmegen PV measurement facility. The temperature was kept at 25 ± 3 °C as measured by a temperature probe on the contact plate. The acquisition was done with 2 ms between points, using a 4 wire measurement probe, from reverse to forward voltage. The external quantum efficiency (EQE) of the tandem cell was measured using a QEXL setup (by PV Measurements) equipped with a grating monochromator, adjustable bias voltage and a bias spectrum.

Room temperature photoluminescence (PL) measurements were done with an excitation wavelength of 785 nm on complete cells using a modified Renishaw Raman spectrometer equipped with a Si CCD detector.

Scanning electron microscopy (SEM) images of the tandem cell structures were acquired using a Zeiss Merlin field emission electron microscope under a 5 kV acceleration voltage.

3 Results and Discussions

3.1 Minority carrier lifetime measurements on Si

The minority carrier lifetime of Si was used as a figure of merit throughout the paper to evaluate the bottom cell after CZTS and tandem cell processing. For this purpose, 10 symmetrically passivated wafers with an initial mean lifetime of 2.65 ± 0.52 ms were prepared. By having a uniform surface passivation quality across the wafer set, we ensure that the passivation properties are not a variable in the subsequent studies. More details on the passivation statistics are shown in the supplementary information (**Fig. S1**). Three different set of samples were prepared, as listed in **Table 1** and illustrated in **Fig. 1**. All the samples have a 25 nm TiN layer at the backside, to eliminate any unwanted contamination from that side during the different processing steps.

Table 1 – Overview of the different samples used for minority carrier lifetime measurements. Note: all the samples have 25 nm TiN on the backside.

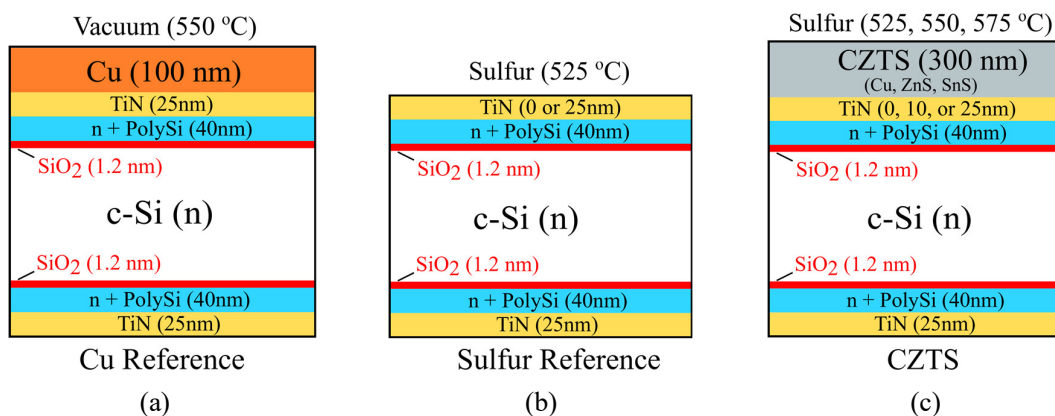| Sample	TiN thickness (nm)	Annealing atmosphere/T (℃)	Purpose
Cu Reference	25	Vacuum/550	Compare metallic Cu to Cu in CZTS
Sulfur Reference	0, 10	Sulfur/525	Isolate the effect of S
CZTS	0, 10, 25	Sulfur/525, 550, 575	Integration of CZTS on Si

Fig. 1 – Cross-section scheme of the samples used for minority carrier lifetime measurements: a) Cu reference, b) Sulfur reference and c) CZTS.

In **Fig. 2**, the Si minority carrier lifetime results of the Cu Reference sample are shown. This case shows that TiN barrier layer fails after a 15 min annealing at 550 ℃, with a 73% loss in lifetime. The lifetime is further degraded when the annealing time is increased. These results indicate that, for this temperature range, the 25 nm TiN barrier layer was not enough to protect the sample against Cu diffusion.
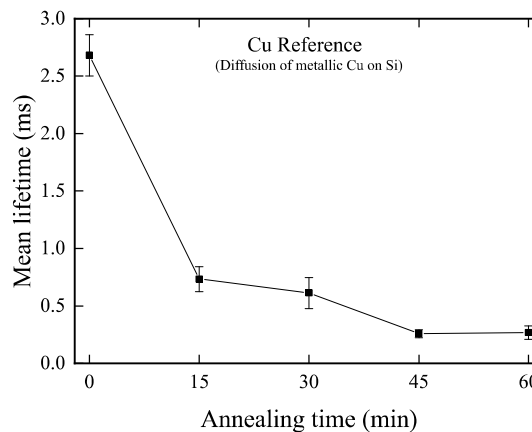

Fig. 2 – Minority carrier lifetime evolution of the Cu Reference sample as the annealing time increases at 550 ℃ in vacuum.

In **Fig. 3 (a)** and **(b)**, the Si carrier lifetime results for the Sulfur Reference and CZTS cases are shown. Here, the lifetime was also monitored after each major processing step, namely the TiN deposition and the CZTS annealing steps. From the "As-Passivated" to the "Before TiN" step, there was a waiting time on the order of a few weeks, causing a slight decrease in the lifetime value due to ageing. This was also monitored before conducting the subsequent experiments. The final lifetimes of **Fig. 3 (a)** are reduced to 45-50% of the "As-passivated" value after annealing in a sulfur atmosphere, suggesting the role of S as a contaminating species. The 60 min point of the Cu reference carrier lifetime of **Fig. 2** is included in **Fig. 3 (a)** for comparison, showing that the impact of the S atmosphere is less severe than that of metallic Cu. Further details and mappings on the Cu Reference and Sulfur Reference carrier lifetime measurements are shown in the supplementary **Fig. S2** and **Fig. S3**, respectively.

In **Fig. 3 (b)**, the key observation is that the final lifetime values after CZTS processing are significantly higher than the Cu Reference case, in spite of the fact that metallic Cu is present as one of the co-sputtered CZTS precursors. One possible explanation for this milder contamination effect is that the driving force for the formation of $Cu_{2-x}S$ phases (the binary phases in the CZTS phase diagram with the lowest melting point [26]) competes directly with the diffusion of the available Cu into Si. Moreover, the lifetime values after CZTS processing are comparable to the Sulfur Reference case, indicating that having CZTS in addition to a sulfur atmosphere does not lead to additional lifetime deterioration.
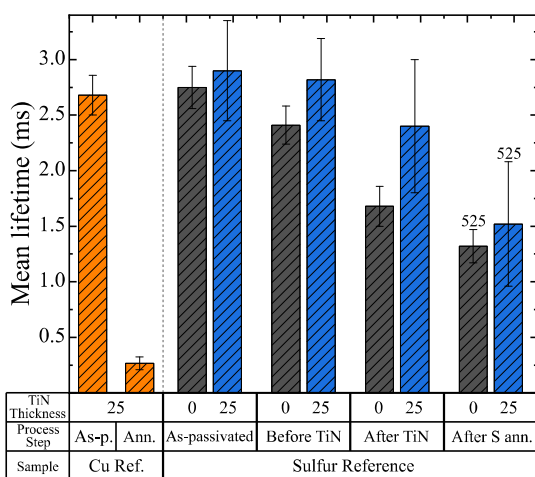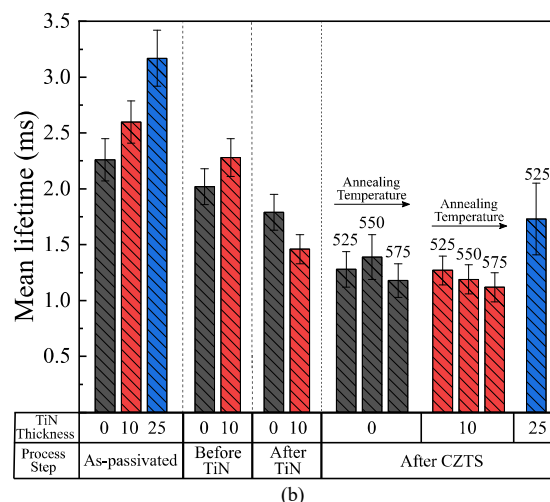
Fig. 3 – Mean effective minority carrier lifetimes of Si for (a) the Cu Reference and Sulfur Reference samples, and (b) the CZTS-processed samples, at each different processing step. The temperatures of the annealing series (in ℃) are indicated above the corresponding bars. Note: All the samples have 25 nm TiN on the backside, so they all show some "After TiN" degradation.

The influence of the annealing temperature was also studied in the CZTS case with a series of different annealing temperatures at 525 ℃, 550 ℃ and 575 ℃, for the cases without TiN and 10 nm TiN, as shown in the "After CZTS" step of **Fig. 3 (b)**. One single measurement with a TiN thickness of 25 nm is included as reference for comparison in the subsequent studies. However, this thickness would be too high for use in a tandem cell (due to poor transparency). The annealing series shows that while the 10 nm TiN case seems to follow a trend with increasing temperature, this is not true for the case without TiN. This is likely due to spatial variations in the sample's lifetime, shown by the uncertainty bars, which have a size comparable to the variations seen in the temperature series. Moreover, it can be seen that the 0 nm and 10 nm TiN series have comparable absolute carrier lifetimes after CZTS processing. To further understand this behavior, in **Fig. 4** we plot the same results but scaling them relative to the respective "After TiN" lifetime value. By doing this, it becomes clearer that the lifetime deterioration during CZTS processing is more significant when no TiN is present. This procedure is also justified as it can be noted in both **Fig. 3 (a)** and **(b)** that the final (post-process) lifetime values are affected by a significant and non-uniform loss in lifetime during the TiN deposition step. The reason for this loss is unknown and still under investigation.
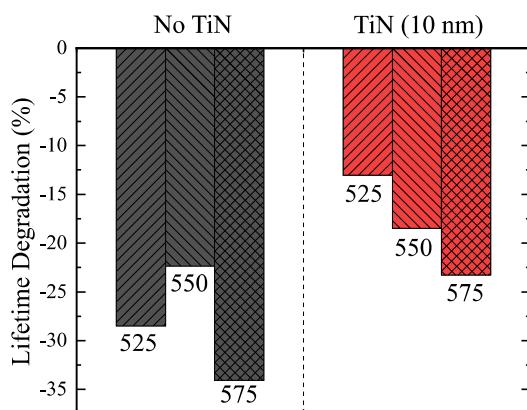
Fig. 4 – Relative change in minority carrier lifetime for the annealing series in the CZTS-processed samples, when scaled to the respective "After TiN" lifetime values. The temperature is displayed on the bars (in °C).

Fig. 5 – Comparison between the i-V_{oc} of a CZTS processed sample, annealed in a sulfur atmosphere at 525 °C for 30 min (in red), and a reference without CZTS processing (in grey). Both half-wafers are cleaved from the same substrate, and are end-passivated with 40 nm Al_2O_3 on both sides after etching the TiN and CZTS layers.

Despite the degradation throughout the processing, the end lifetimes are above 1 ms, which corresponds to an i-V_{oc} above 700 mV. This encouraging result indicates that the performance of the bottom silicon cell may not necessarily be compromised as a result of the CZTS synthesis. However, given the comparable absolute lifetime values, regardless of the TiN thickness, it is not yet clear from these results alone whether the use of a TiN barrier layer would be useful.

To further evaluate whether the observed degradation is related to a bulk contamination or TO/n+polySi surface de-passivation, a complementary experiment was conducted where a silicon wafer was passivated only at the end of the CZTS processing, after etching the CZTS and TiN layers. Additionally, any possible unforeseen effects caused by the TO/n+polySi passivation are avoided by using this configuration. We refer to this as the "end-passivated" sample. Here, we repeated the Si/TiN(25nm)/CZTS sample, except using a non-passivated bare silicon wafer (no TO/n+polySi passivation) as the substrate. Subsequent to the CZTS and TiN etching and cleaning, a 40 nm Al_2O_3 layer was deposited on both sides for surface passivation. The results, plotted in **Fig. 5**, indicate a tolerable 16 mV decrease in i-V_{oc} (20% decrease in lifetime) for the sample with CZTS processing compared to the clean reference sample.

Even though this experiment does not directly clarify the effect of the polySi layer on the diffusion of contaminants from CZTS processing, it shows that relatively high-end lifetimes can be achieved without using a polySi layer. This suggests that there is some flexibility of design in the bottom Si cell, and offers new perspectives for future tandem integration experiments.
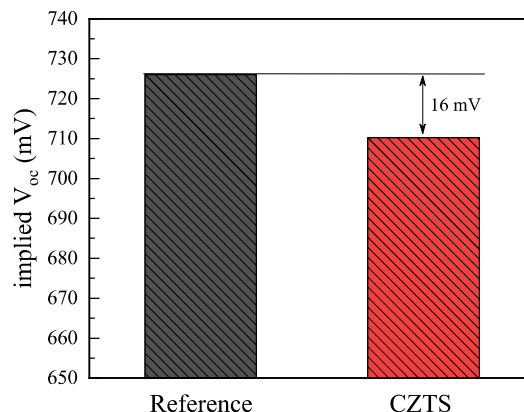
3.2 SIMS and RBS Analysis

To correlate the lifetime results with possible diffusion of contaminants into the Si bulk, SIMS and RBS measurements were performed on selected Cu Reference and CZTS-processed samples (after etching of the Cu, TiN and CZTS layers). The SIMS results are illustrated in **Fig. 6**. For the Cu Reference samples, the corresponding quantitative Cu SIMS depth profiles are shown in **Fig. 6 (a)**. A clear diffusion tail into the c-Si bulk is detected in all cases, with a Cu peak concentration of up to 10^{20} cm^{-3} occurring in the polySi. Furthermore, an increase in Cu concentration is seen with increasing annealing time, which is in qualitative agreement with the lifetime results of **Fig. 2**. In **Fig. 6 (b)**, a quantitative Cu profile is presented for the CZTS-processed samples annealed at 525 °C. The Cu profiles reveal that for the No TiN and 10 nm TiN samples, there is a diffusion tail extending at least 100 nm into the Si bulk, but for the 25 nm TiN case the Cu concentration drops sharply to below detection limits after the polySi. In all three cases, the Cu concentration is 2-3 orders of magnitude lower compared to the Cu reference case, which helps to justify their significantly higher lifetimes. Into the Si bulk (close to the surface), the Cu concentration is always lower than 10^{18} cm^{-3}, which in Si corresponds to 0.002 at% (or 20 ppm).

Depth profiles of other relevant elements during CZTS processing, namely Zn, Sn, S and Ti (from TiN) are shown in **Fig. 6 (c)** to **(f)**. Other elements than Cu appear to be at background levels or near detection limits into the c-Si bulk. Further quantification of these elements is provided next, following the RBS measurements.
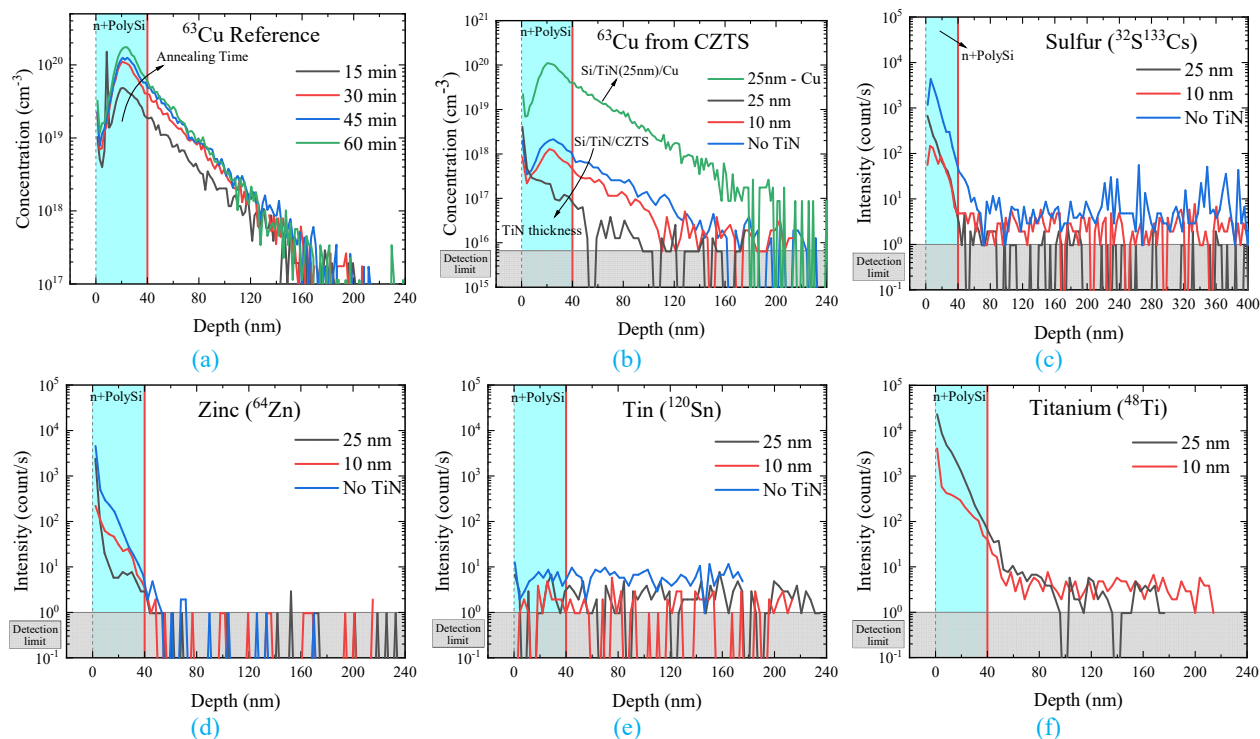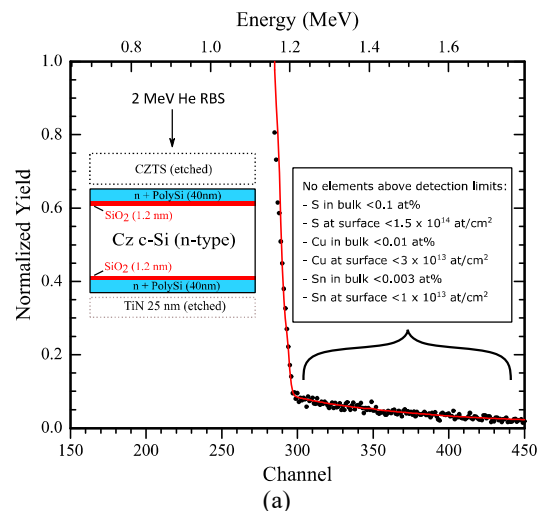
Fig. 6 –SIMS depth profiles for Cu Reference and CZTS-processed samples. (a) The Cu reference, showing quantitative Cu depth profiles; (b) Quantitative Cu depth profile for the CZTS-processed samples. The depth profile of the Cu Reference sample is added for comparison; (c), (d), (e) and (f) Qualitative depth profiles of Zn, Sn, S, and Ti for the CZTS samples, respectively. The measurements are performed on the n+polySi layer towards the c-Si bulk, as marked by the blue rectangle. The CZTS-processed samples were annealed at 525 °C. The annealing time was 30 min unless otherwise specified.

To complement the SIMS analysis, RBS measurements were done on the CZTS-processed samples with 0 nm and 10 nm TiN, annealed at 525 °C. The results are illustrated in **Fig. 7 (a)** and **(b)**, respectively. As all the potential contaminant elements are heavier than Si, the RBS data is zoomed in at energies higher than the Si onset. It can be seen that none of the possible contaminants are detected in Si, other than some Ti at the surface, which was not fully removed during the piranha etching (this was confirmed with SEM, not shown here). This means that an estimate for the upper limit for the concentration of these contaminants can be established, and is given by the sensitivity of the measurement itself. For the measurement conditions of **Fig. 7 (a)** and **(b)**, these upper limits are given in the figure insets. In the particular case of Cu, which was also quantitatively measured by SIMS, RBS dictates that its concentration has to be below 0.01 at%, agreeing with the value of below 0.002 at% given by SIMS.
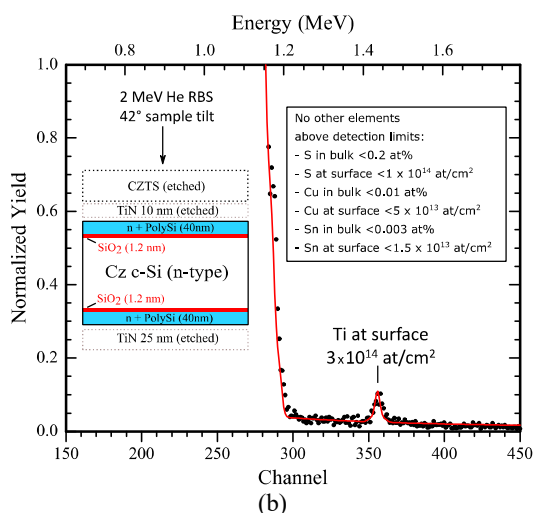
Energy (MeV)

2 MeV He RBS
42° sample tilt

CZTS (etched)
TiN 10 nm (etched)
n + PolySi (40nm)
SiO₂ (1.2 nm)
Cz c-Si (n-type)
SiO₂ (1.2 nm)
n + PolySi (40nm)
TiN 25 nm (etched)

No other elements
above detection limits:
- S in bulk <0.2 at%
- S at surface <1 x 10^{14} at/cm²
- Cu in bulk <0.01 at%
- Cu at surface <5 x 10^{13} at/cm²
- Sn in bulk <0.003 at%
- Sn at surface <1.5 x 10^{13} at/cm²

Ti at surface
3×10^{14} at/cm²

(b)

Fig. 7 –RBS results for the CZTS-processed samples with (a) No TiN and (b) 10 nm TiN. The insets show the structures used and the detection limits for the contaminant elements. The samples were annealed at 525 ℃

3.3 DLTS Analysis

To further assess the influence of these possible contaminants, DLTS measurements were made on CZTS-processed samples annealed at 525 ℃. Here, samples without the TO/n+polySi passivation were prepared as no Schottky contact (required in our DLTS setup) could be obtained between the metal electrode and the heavily-doped polySi. An unprocessed bare "Reference" wafer was also included to rule out any possible pre-existing defects. The results are plotted in **Fig. 8**. It is shown that the samples with 10 nm TiN, 25 nm TiN and the Reference wafer do not have any DLTS signal, but the No TiN sample exhibits peaks related to electrically active defects, with two features peaking at ~175 K and ~275 K. The 175 K peak shows a broadening towards the lower temperature side, which may be related to several overlapping defect signatures or extended defects [62]. In the case of extended defects, an exponential decay in emission rate may not hold, and will influence the extracted activation energies and apparent capture cross sections from an Arrhenius plot of the corresponding DLTS peak [63]. This peak near 175 K might come from several defects associated with precipitates of Cu [39], [64], but further measurements would be required to assign this unambiguosly. The peak at 275 K could be used instead for making an Arrhenius plot. This peak has a broad shape due to its very low capture cross-section of 2×10^{-22} cm², and its energy level was found to be 0.16 eV below the conduction band edge, as extracted from the Arrhenius plot. The level at $E_c - 0.16$ eV has previously been reported in Cu diffused Si and showed to originate from interstitial copper or a complex of interstitial copper by Istratov *et al* [65]. More

details on the DLTS results, analysis and Arrhenius plot can be found in the supplementary information (**Fig. S4** and **Fig. S5**).
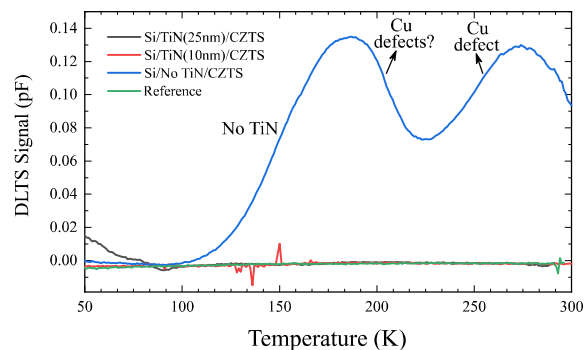

Fig. 8 –DLTS results of CZTS-processed samples annealed at 525 ℃ compared to a clean reference Si wafer. Note: these DLTS samples do not contain the TO/n+polySi passivation stack.

Based on these findings, a 10 nm TiN seems to be sufficient to prevent the formation of electrically active defects in the Si bulk. This thickness was thus selected to prepare a full CZTS/Si tandem solar cell.

3.4 Fabrication of a monolithic CZTS/Si solar cell

The effective minority carrier lifetime of the silicon bottom cell was monitored at different steps of the fabrication process, as in **Section 3.1**. However, the samples are now asymmetrically passivated (with TO/p+polySi on the backside), and an additional SiN hydrogenation step (to improve the passivation quality) is also included. The corresponding i-V_{oc} changes of the silicon cell is shown in **Fig. 9**. It can be seen in **Fig. 9** that the i-V_{oc} of the silicon bottom cell was slightly degraded after the TiN deposition step, while this value does not degrade further during the full fabrication of the CZTS top cell. This demonstrates that the 10 nm TiN has been effective as the diffusion barrier. The J-V characteristic curve, EQE and schematic illustration of the tandem device are shown in **Fig. 10 (a), (b)** and **(c)**, respectively.
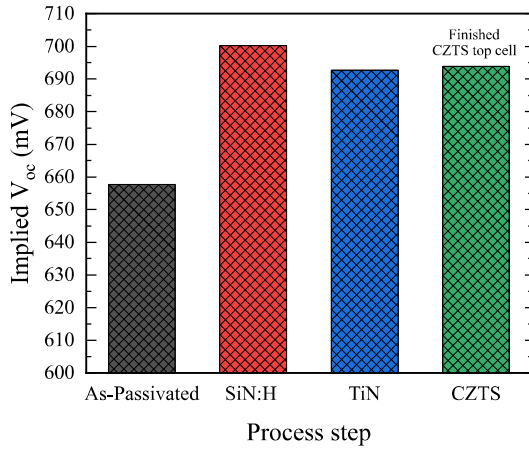
Fig. 9 – Changes in i-V_{oc} of the silicon bottom cell during the fabrication processes of the CZTS/Si tandem cell. The indicated fabrication steps are: 1) Silicon surface passivation 2) SiN:H hydrogenation of the TOPCon layers 3) TiN deposition, and 4) Full CZTS cell fabrication before depositing the Ag back contact.

As seen in **Fig. 10** (a), the tandem cell shows a V_{oc} of 899 mV, which is higher than the values expected for each individual junction separately, when produced under the same conditions (as shown in the supplementary **Fig. S6** and **Fig. S7**). However, it exhibits a low efficiency of 1.10%, and the light J-V curve exhibits a clear "rollover" effect, which is characterized by a distortion of the J-V curve, causing a very low FF.

This rollover effect has been reported previously for non-optimal tandem cells, and was associated with the reverse breakdown voltage regime of the top cell when the tandem is current-mismatched [66]. While this explanation is certainly plausible here, we note that other effects have been identified that can cause a rollover effect in single-junction solar cells. This occurs when there is one or more barriers to current extraction throughout the solar cell under illumination. This can be due to the presence of Schottky diodes in non-ohmic contacts (namely the n+ polySi/TiN or TiN/CZTS interfaces), or a non-ideal p-n junction, leading to a voltage-dependent current blocking behavior. In particular, this has been reported for non-ideal p-n junctions in single-junction CZTS cells [67], and we have also seen it in our internal experiments for CZTS/CdS p-n junctions when the synthesis parameters are not ideal (see supplementary **Fig. S8**). In the case of Si, we found evidence that a 10 nm TiN layer can cause a roll-over behavior on single junction Si cells alone (see supplementary **Fig. S9**). Furthermore, a rollover effect has been reported in CIGS at the Mo/CIGS interface in non-glass substrates, where there is no natural inclusion of Na (or other alkali elements) in the absorber layer. It was shown that this effect can be completely eliminated by providing a sufficient amount of Na [68]. This is particularly relevant in this work, as the growth of CZTS is also substrate dependent, and no intentional Na was added in the fabrication of the tandem cell.
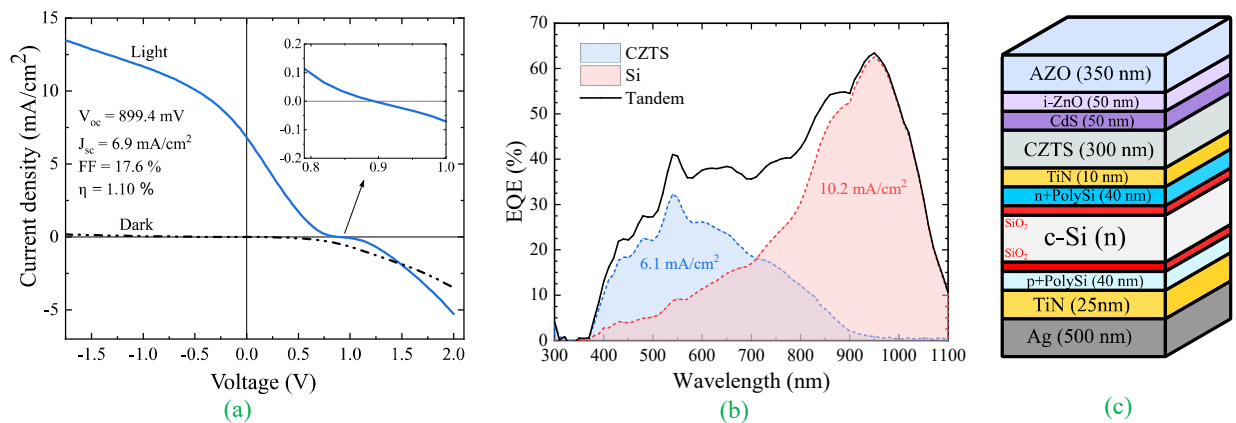

Fig. 10 – (a) Tandem cell illuminated (solid) and dark (dashed) J-V curves. The insets show region near Voc and the J-V parameters; (b) EQE of the two subcells and sum of the subcell contributions; (c) Tandem solar cell scheme.

To explore these issues, we compare the results of our tandem device to a baseline single-junction CZTS cell where the CZTS thickness was reduced from the typical 1 µm to a value of around 275 nm, similar to the value used for the tandem. This "thin CZTS cell" achieved an efficiency of 5.8%, with a J_{sc} of 15.8 mA/cm² and a V_{oc} of

585 mV (a J-V curve is shown in the supplementary **Fig. S9**), which is fairly comparable to state of the art thin CZTS devices (with a record of 8.57% for a 400 nm thick CZTS [69]). However, when compared to the CZTS growth for the tandem cell, significant morphological differences between the two CZTS layers are noticeable. A morphology comparison is presented in **Fig. 11**. The top

views in **Fig. 11 (a)** and **(b)** show a clear difference in grain size. The tandem cell cross-section, in **Fig. 11 (c),** shows that the CZTS exhibits a double layer structure, with a smaller grain size. In comparison, the CZTS grown with the same conditions on Mo-coated soda lime glass (SLG), shown in **Fig. 11 (d),** has a single layer and larger grains. This indicates that the local conditions for CZTS growth are different in the two cases. Additionally, CZTS photoluminescence (PL) measurements made on both the fully finished tandem and the thin CZTS cell, confirm that the thin CZTS cell exhibits a significantly higher PL intensity (see supplementary **Fig. S10**). We suggest that one possible reason for these differences is likely to be the contribution of Na diffusion from the glass, which is not available in Si. This possibility will be explored in future work.

The results of this work show that there is a margin for monolithically integrating a CZTS top cell on a full Si bottom cell using high temperature processing above 500 ℃, without compromising the bottom cell. Given the constituting contaminant elements of CZTS (in particular Cu and S), we suggest that this study could be generalized to other thin film chalcogenide materials (many of which do contain Cu), and thereby open up the possibility of exploring new emerging wide band gap semiconductors as top cell alternatives.
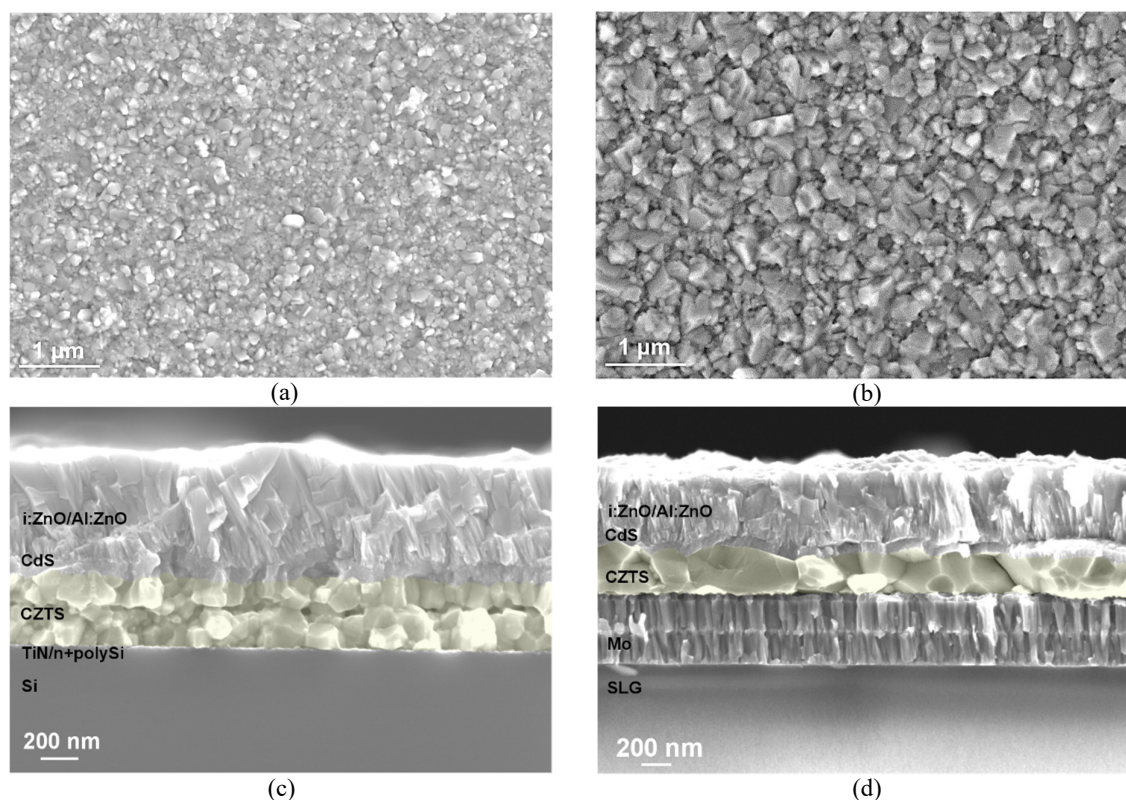

(a)

(b)

(c)

(d)

Fig. 11 –SEM comparison of the tandem cell and a single junction thin CZTS cell. (a) Top view of the CZTS surface as used on the tandem cell, before CdS deposition; (b) Top view of the thin CZTS surface, before CdS deposition; (c) Cross section view of the upper part of the tandem; (d) Cross section view of the full thin CZTS cell. The CZTS absorber layer is highlighted in yellow.

4 Conclusion

In this work, we have assessed the potential of monolithically-integrated two-terminal tandem cells based on thin-film chalcogenides on Si, using CZTS and double-side TOPCon Si. We have investigated the use of a thin TiN barrier layer to protect the bottom Si cell from in-diffusion of metals or sulfur during the CZTS growth, and to serve as interface recombination layer between the top and bottom cells. It was revealed that the degree of Cu contamination induced by CZTS growth on the Si bulk is significantly smaller when compared to a case where metallic Cu is deposited on Si. While traces of all the elements (except for Sn) can be detected at the surface of c-Si after CZTS annealing, it was shown that the biggest contributor to a decrease in the lifetime of the bottom Si

cell is the Cu. Furthermore, it was shown that a TiN barrier layer as thin as 10 nm can effectively suppress the formation of deep Cu-related defects on Si. Based on these results, we presented a proof-of-concept monolithically integrated CZTS/Si tandem solar cell with an efficiency of 1.1% and showing an additive effect on the V_{oc}, reaching 900 mV. The i-V_{oc} of the silicon bottom cell was retained during the full fabrication of the CZTS cell when a 10 nm TiN barrier was used. It is suggested that the poor performance of the tandem cell is mainly due to limitations in the CZTS top cell, namely difficulty of reproducing high-quality CZTS absorbers on non-glass substrates, with unavailability of Na. The possibility of non ohmic blocking behavior at the TiN layer is also mentioned.

By showing that a full TOPCon Si solar cell can be processed at temperatures well above 500 °C in the presence of several critical contaminant elements – notably copper, without suffering from a severe degradation in lifetime and without forming deep defect levels, this work opens up the possibility of exploring other less known and future high bandgap compounds processed at high temperatures. This could allow for achieving high efficiency monolithically integrated tandem solar cells in the future.

5 References

[1]   M. Woodhouse *et al.*, "On the Path to SunShot: The Role of Advancements in Solar Photovoltaic Efficiency, Reliability, and Costs," *National Renewable Energy Laboratory (NREL)*. 2016.

[2]   VDMA, "International Technology Roadmap for Photovoltaic (ITRPV): Results 2017 Including maturity report 2018." 2018.

[3]   Markus Fischer, "ITRPV 10th edition 2019 - report release and key findings," 2019.

[4]   W. Shockley and H. J. Queisser, "Detailed Balance Limit of Efficiency of p-n Junction Solar Cells," *J. Appl. Phys.*, vol. 32, no. 3, pp. 510–519, Mar. 1961.

[5]   M. A. Green, *Solar cells: Operating principles, technology and system applications*. Prentice-Hall Inc., 1982.

[6]   M. A. Green, "Silicon wafer-based tandem cells: The ultimate photovoltaic solution?," in *Proc. of SPIE*, 2014, vol. 8981, p. 89810L.

[7]   Z. (Jason) Yu, M. Leilaeioun, and Z. Holman, "Selecting tandem partners for silicon solar cells," *Nat. Energy*, vol. 1, no. 11, p. 16137, 2016.

[8]   S. Essig *et al.*, "Raising the one-sun conversion efficiency of III–V/Si solar cells to 32.8% for two junctions and 35.9% for three junctions," *Nat. Energy*, vol. 2, no. 9, p. 17144, Aug. 2017.

[9]   M. A. Green *et al.*, "Solar cell efficiency tables (Version 53)," *Prog. Photovoltaics Res. Appl.*, vol. 27, no. 1, pp. 3–12, Jan. 2019.

[10]   Sharp Corporation, "Sharp Develops Solar Cell with World's Highest Conversion Efficiency of 37.9%," 2013. [Online]. Available: http://www.sharp-world.com/corporate/news/130424.html. [Accessed: 05-Apr-2019].

[11]   P. Iles, "Evolution of space solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 68, no. 1, pp. 1–13, Apr. 2001.

[12]   M. Yamaguchi, T. Takamoto, and K. Araki, "Present and future of super high efficiency multi-junction solar cells," in *Proceedings of SPIE, the*, 2008, vol. 6889, no. February 2008, p. 688906.

[13]   T. Todorov, O. Gunawan, and S. Guha, "A road towards 25% efficiency and beyond: perovskite tandem solar cells," *Mol. Syst. Des. Eng.*, vol. 1, no. 4, pp. 370–376, 2016.

[14]   F. Sahli *et al.*, "Fully textured monolithic perovskite/silicon tandem solar cells with 25.2% power conversion efficiency," *Nat. Mater.*, Jun. 2018.

[15]   Oxford PV, "Oxford PV perovskite solar cell achieves 28% efficiency," 2018. [Online]. Available: https://www.oxfordpv.com/news/oxford-pv-perovskite-solar-cell-achieves-28-efficiency. [Accessed: 12-Jan-2019].

[16]   "Best Research-Cell Efficiencies," no. 12-18–2018. NREL, 2018.

[17]   J. W. Garland, T. Biegala, M. Carmody, C. Gilmore, and S. Sivananthan, "Next-generation multijunction solar cells: The promise of II-VI materials," *J. Appl. Phys.*, vol. 109, no. 10, 2011.

[18]   C. Yan *et al.*, "Cu2ZnSnS4 solar cells with over 10% power conversion efficiency enabled by heterojunction heat treatment," *Nat. Energy*, vol. 3, no. 9, pp. 764–772, Sep. 2018.

[19]   S. Oueslati *et al.*, "Effect of germanium incorporation on the properties of kesterite Cu2ZnSn(S,Se)4 monograins," *Thin Solid Films*, vol. 669, no. June 2018, pp. 315–320, 2019.

[20]   E. Garcia-Llamas *et al.*, "Wide band-gap tuning Cu2ZnSn1−xGexS4 single crystals: Optical and vibrational properties," *Sol. Energy Mater. Sol. Cells*, vol. 158, pp. 147–153, Dec. 2016.

[21]   M. Umehara, S. Tajima, Y. Takeda, and T. Motohiro, "Wide bandgap Cu 2 ZnSn 1−x Ge x S 4 fabricated on transparent conductive oxide-coated substrates for top-cells of multi-junction solar cells," *J. Alloys Compd.*, vol. 689, pp. 713–717, Dec. 2016.

[22]   W. Gong, T. Tabata, K. Takei, M. Morihama, T. Maeda, and T. Wada, "Crystallographic and optical properties of (Cu, Ag) 2 ZnSnS 4 and (Cu, Ag) 2 ZnSnSe 4 solid solutions," *Phys. status solidi*, vol. 12, no. 6, pp. 700–703, Jun. 2015.

[23]   G. Sai Gautam, T. P. Senftle, and E. A. Carter, "Understanding the Effects of Cd and Ag Doping in Cu 2 ZnSnS 4 Solar Cells," *Chem. Mater.*, vol. 30, no. 14, pp. 4543–4555, Jul. 2018.

[24]   H. Cui, X. Liu, F. Liu, X. Hao, N. Song, and C. Yan, "Boosting Cu2ZnSnS4 solar cells efficiency by a thin Ag intermediate layer between absorber and back contact," *Appl. Phys. Lett.*, vol. 104, no. 4, pp. 2–6, 2014.

[25]   S. Adachi, *Earth-Abundant Materials for Solar Cells: Cu2-II-IV-VI4 Semiconductors*. John Wiley & Sons, Ltd, 2015.

[26]   K. Ito, *Copper Zinc Tin Sulfide-Based Thin Film Solar Cells*. John Wiley & Sons, Ltd, 2015.

[27]   K. Oishi *et al.*, "Growth of Cu2ZnSnS4 thin films on Si (100) substrates by multisource evaporation," *Thin Solid Films*, vol. 517, no. 4, pp. 1449–1452, 2008.

[28]   B. Shin, Y. Zhu, T. Gershon, N. A. Bojarczuk, and S.

Guha, "Epitaxial growth of kesterite Cu2ZnSnS4 on a Si(001) substrate by thermal co-evaporation," *Thin Solid Films*, vol. 556, pp. 9–12, 2014.

[29]   N. Song *et al.*, "Epitaxial Cu2ZnSnS4 thin film on Si (111) 4° substrate," *Appl. Phys. Lett.*, vol. 106, no. 25, p. 252102, 2015.

[30]   E. Mellikov *et al.*, "Monograin materials for solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 93, no. 1, pp. 65–68, Jan. 2009.

[31]   J. Liu, Y. Yao, and S. Xiao, "Interdigitated back contact solar cells with polycrystalline silicon on oxide passivating contacts for both polarities Related content Review of status developments of high-efficiency crystalline silicon solar cells," *Japanese J. Appl. Phys. Regul. Pap.*, 2017.

[32]   F. Feldmann, M. C. Bivour Reichel, M. Hermle, and S. W. Glunz, "A Passivated Rear Contact for High-Efficiency n-Type Si Solar Cells Enabling High Vocs and FF>82%," 2013.

[33]   F. Haase *et al.*, "Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells," 2018.

[34]   F. Feldmann, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, "Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics," *Sol. Energy Mater. Sol. Cells*, vol. 120, pp. 270–274, Jan. 2014.

[35]   F. Feldmann, M. Bivour, C. Reichel, H. Steinkemper, M. Hermle, and S. W. Glunz, "Tunnel oxide passivated contacts as an alternative to partial rear contacts," *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 46–50, Dec. 2014.

[36]   J. B. Heng *et al.*, ">23% High-Efficiency Tunnel Oxide Junction Bifacial Solar Cell With Electroplated Cu Gridlines," *IEEE J. Photovoltaics*, vol. 5, no. 1, pp. 82–86, Jan. 2015.

[37]   M. Rienacker *et al.*, "Junction Resistivity of Carrier-Selective Polysilicon on Oxide Junctions and Its Impact on Solar Cell Performance," *IEEE J. Photovoltaics*, vol. 7, no. 1, pp. 11–18, Jan. 2017.

[38]   F. Feldmann, C. Reichel, R. Müller, and M. Hermle, "The application of poly-Si/SiO x contacts as passivated top/rear contacts in Si solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 159, pp. 265–271, Jan. 2017.

[39]   E. R. Weber, "Impurity Precipitation, Dissolution, Gettering, and Passivation in PV Silicon: Final Technical Report." 2002.

[40]   A. A. Istratov and E. R. Weber, "Electrical properties and recombination activity of copper, nickel and cobalt in silicon," *Appl. Phys. A Mater. Sci. Process.*, vol. 66, no. 2, pp. 123–136, 1998.

[41]   A. A. Istratov and E. R. Weber, "Physics of Copper in Silicon," *J. Electrochem. Soc.*, vol. 149, no. 1, p. G21, 2002.

[42]   M. Seibt, R. Khalil, V. Kveder, and W. Schröter, "Electronic states at dislocations and metal silicide precipitates in crystalline silicon and their role in solar cell materials," *Appl. Phys. A*, vol. 96, no. 1, pp. 235–253, Jul. 2009.

[43]   S. M. Sze and J. C. Irvin, "Resistivity, mobility and impurity levels in GaAs, Ge, and Si at 300°K," *Solid. State. Electron.*, vol. 11, no. 6, pp. 599–602, Jun. 1968.

[44]   A. Masuhr, H. Bracht, N. A. Stolwijk, H. Overhof, and

[45]   H. Mehrer, "Point defects in silicon after zinc diffusion - a deep level transient spectroscopy and spreading-resistance profiling study," *Semicond. Sci. Technol.*, vol. 14, no. 5, pp. 435–440, May 1999.

[45]   C. S. Fuller and F. J. Morin, "Diffusion and electrical behavior of zinc in silicon," *Phys. Rev.*, vol. 105, no. 2, pp. 379–384, 1957.

[46]   A. N. Larsen, "Radiation-induced defects in Ge- and Sn-doped n-type Si," in *Crystalline Defects and Contamination: Their Impact and Control in Device Manufacturing III : DECON 2001 : Proceedings of the Satellite Symposium to ESSDERC 2001, Nuremberg, Germany*, B. O. Kolbesen, Ed. Electrochemical Society, 2001.

[47]   A. Nylandsted Larsen *et al.*, "Tin-vacancy acceptor levels in electron-irradiated n-type silicon," *Phys. Rev. B*, vol. 62, no. 7, pp. 4535–4544, Aug. 2000.

[48]   R. Y. Koyama, W. E. Phillips, D. R. Myers, Y. M. Liu, and H. B. Dietrich, "The energy levels and the defect signature of sulfur-implanted silicon by thermally stimulated measurements," *Solid. State. Electron.*, vol. 21, no. 7, pp. 953–955, Jul. 1978.

[49]   Y. Mo, M. Z. Bazant, and E. Kaxiras, "Sulfur point defects in crystalline and amorphous silicon," *Phys. Rev. B*, vol. 70, no. 20, p. 205210, Nov. 2004.

[50]   N. Song, J. Chen, C. Yan, X. Wen, X. Hao, and M. A. Green, "Effect of a ZnS intermediate layer on properties of Cu2ZnSnS4 films from sputtered Zn/CuSn precursors on Si (100) substrate," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, 2016, no. 00, pp. 1516–1518.

[51]   A. E. Kaloyeros and E. Eisenbraun, "Ultrathin Diffusion Barriers/Liners for Gigascale Copper Metallization," *Annu. Rev. Mater. Sci.*, vol. 30, no. 1, pp. 363–385, Aug. 2000.

[52]   C. Lee and Y.-L. Kuo, "The evolution of diffusion barriers in copper metallization," *JOM*, vol. 59, no. 1, pp. 44–49, Jan. 2007.

[53]   S. Oueslati *et al.*, "Study of alternative back contacts for thin film Cu 2 ZnSnSe 4 -based solar cells," *J. Phys. D. Appl. Phys.*, vol. 48, no. 3, p. 035103, Jan. 2015.

[54]   T. Schnabel and E. Ahlswede, "On the interface between kesterite absorber and Mo back contact and its impact on solution-processed thin-film solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 159, pp. 290–295, 2017.

[55]   S. Englund *et al.*, "Characterization of TiN back contact interlayers with varied thickness for Cu2ZnSn(S,Se)4 thin film solar cells," *Thin Solid Films*, vol. 639, pp. 91–97, 2017.

[56]   B. Shin, Y. Zhu, N. A. Bojarczuk, S. Jay Chey, and S. Guha, "Control of an interfacial MoSe 2 layer in Cu 2 ZnSnSe 4 thin film solar cells: 8.9% power conversion efficiency with a TiN diffusion barrier," *Appl. Phys. Lett.*, vol. 101, no. 5, p. 053903, Jul. 2012.

[57]   J. J. Scragg, T. Kubart, J. T. Wätjen, T. Ericson, M. K. Linnarsson, and C. Platzer-Björkman, "Effects of back contact instability on Cu2ZnSnS4 devices and processes," *Chem. Mater.*, vol. 25, no. 15, pp. 3162–3171, 2013.

[58]   M. Espindola-Rodriguez *et al.*, "Bifacial Kesterite Solar Cells on FTO Substrates," *ACS Sustain. Chem. Eng.*, vol. 5, no. 12, pp. 11516–11524, 2017.

[59]   A. Cuevas and R. A. Sinton, "Prediction of the open-circuit voltage of solar cells from the steady-state

photoconductance," *Prog. Photovoltaics Res. Appl.*, vol. 5, no. 2, pp. 79–90, 1997.

[60]   L. R. Doolittle, "A semiautomatic algorithm for rutherford backscattering analysis," *Nucl. Instruments Methods Phys. Res. Sect. B Beam Interact. with Mater. Atoms*, vol. 15, no. 1–6, pp. 227–231, Apr. 1986.

[61]   B. G. Svensson, K. -H. Rydén, and B. M. S. Lewerentz, "Overlapping electron traps in n -type silicon studied by capacitance transient spectroscopy," *J. Appl. Phys.*, vol. 66, no. 4, pp. 1699–1704, Aug. 1989.

[62]   W. Schroter, J. Kronewitz, U. Gnauert, F. Riedel, and M. Seibt, "Bandlike and localized states at extended defects in silicon."

[63]   N. Torazawa, S. Hirao, S. Kanayama, H. Korogi, and S. Matsumoto, "The Development of Cu Filling and Reliability Performance with Ru-Ta Alloy Barrier for Cu Interconnects," *J. Electrochem. Soc.*, vol. 163, no. 6, pp. E173–E178, 2016.

[64]   M. Nakamura and S. Murakami, "Deep-Level Transient Spectroscopy and Photoluminescence Studies of Formation and Depth Profiles of Copper Centers in Silicon Crystals Diffused with Dilute Copper," *Jpn. J. Appl. Phys.*, vol. 49, no. 7, p. 071302, Jul. 2010.

[65]   A. A. Istratov, H. Hieslmair, C. Flink, T. Heiser, and E. R. Weber, "Interstitial copper-related center in n-type silicon," *Appl. Phys. Lett.*, vol. 71, no. 16, pp. 2349–2351, Oct. 1997.

[66]   M. Schnabel *et al.*, "Monolithic Si nanocrystal/crystalline Si tandem cells involving Si nanocrystals in SiC," *Prog. Photovoltaics Res. Appl.*, vol. 24, no. 9, pp. 1165–1177, Sep. 2016.

[67]   J. K. Larsen *et al.*, "Cadmium Free Cu2ZnSnS4 Solar Cells with 9.7% Efficiency," *Adv. Energy Mater.*, vol. 1900439, p. 1900439, Apr. 2019.

[68]   R. Caballero *et al.*, "Influence of Na on Cu(In,Ga)Se 2 solar cells grown on polyimide substrates at low temperature: Impact on the Cu(In,Ga)Se 2 /Mo interface," *Appl. Phys. Lett.*, vol. 96, no. 9, pp. 1–4, 2010.

[69]   F. Liu *et al.*, "Beyond 8% ultrathin kesterite Cu2ZnSnS4 solar cells by interface reaction route controlling and self-organized nanopattern at the back contact," *NPG Asia Mater.*, vol. 9, no. 7, p. e401, 2017.